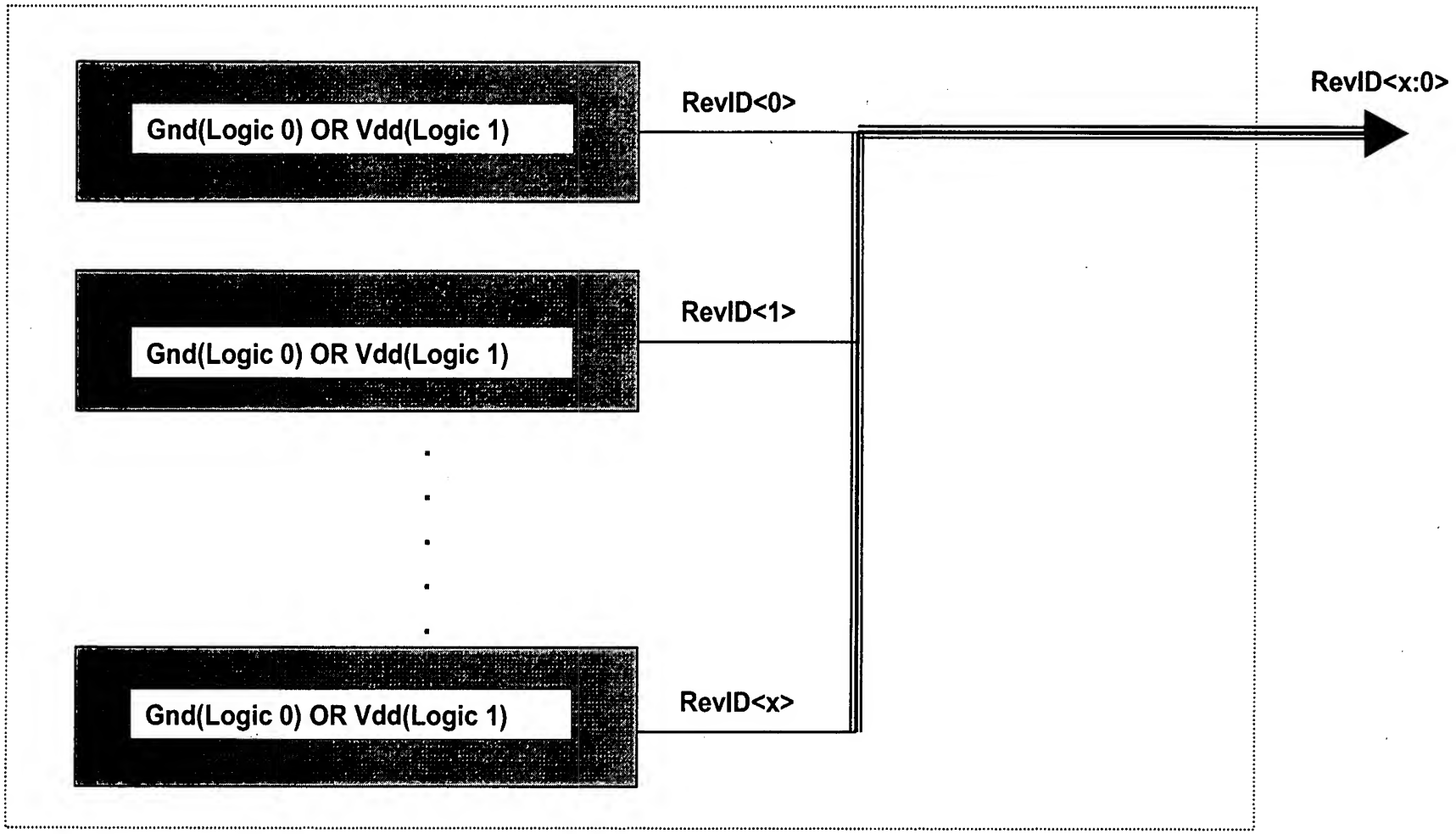

Gnd(Logic 0) OR Vdd(Logic 1)
RevID<0>
RevID<x:0>
Gnd(Logic 0) OR Vdd(Logic 1)
RevID<1>
Gnd(Logic 0) OR Vdd(Logic 1)
RevID<x>

FIG. 1

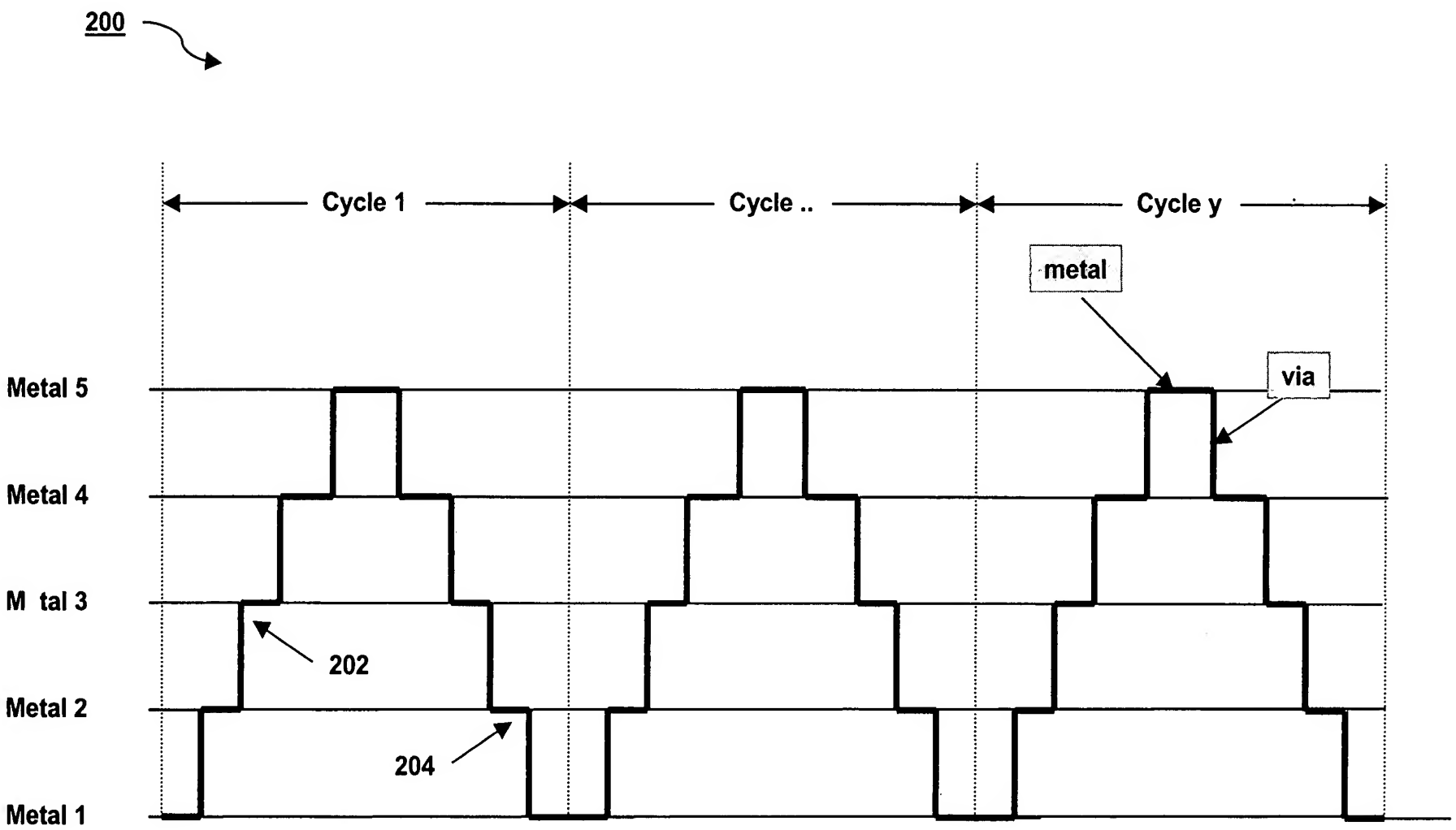

200
Cycle 1
Cycle ..
Cycle y
metal
via
Metal 5
Metal 4
M tal 3
Metal 2
Metal 1
202
204

FIG. 2

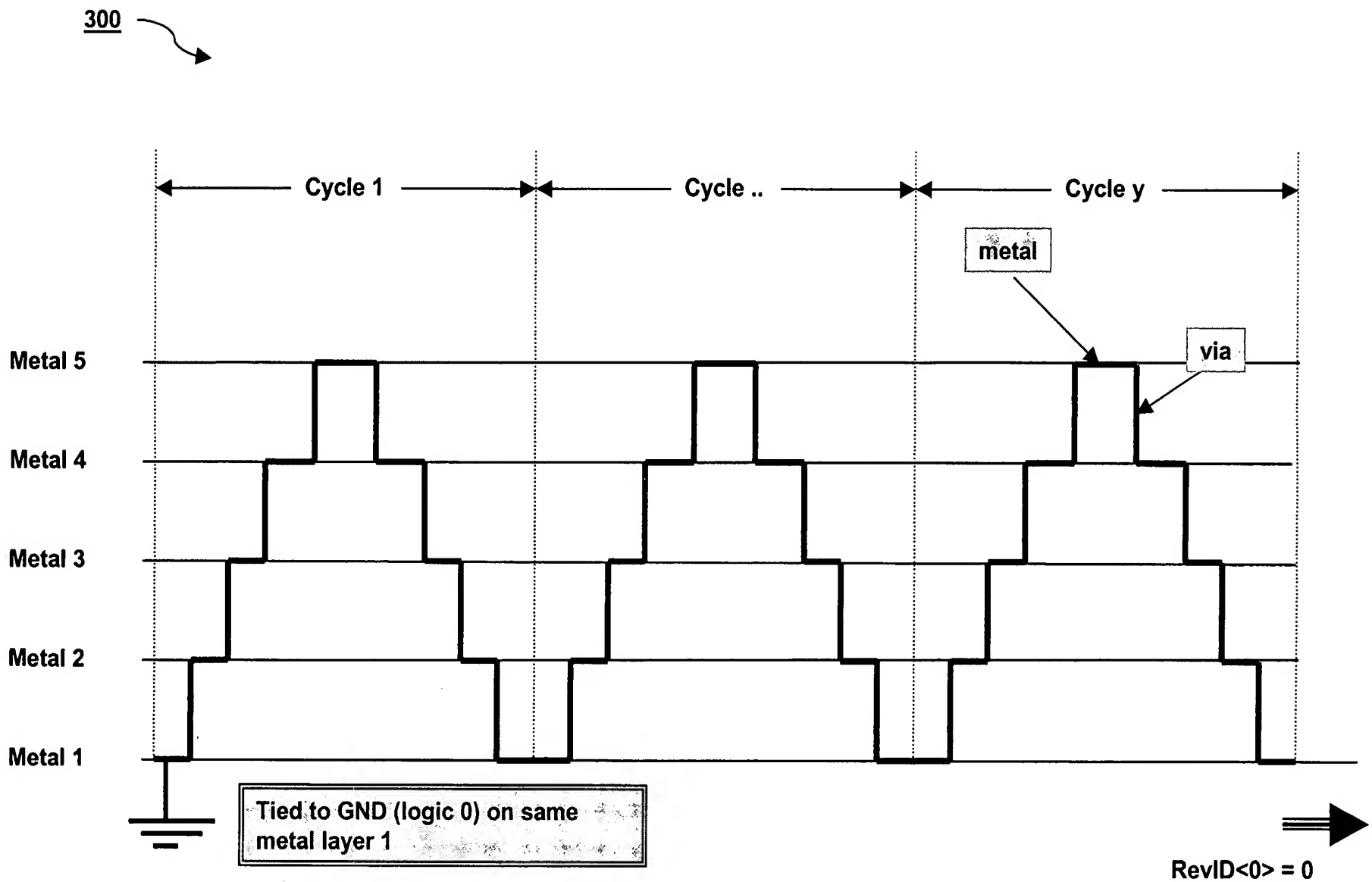

300
Cycle 1
Cycle ..
Cycle y
metal
via
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Tied to GND (logic 0) on same metal layer 1
RevID<0> = 0

FIG. 3A

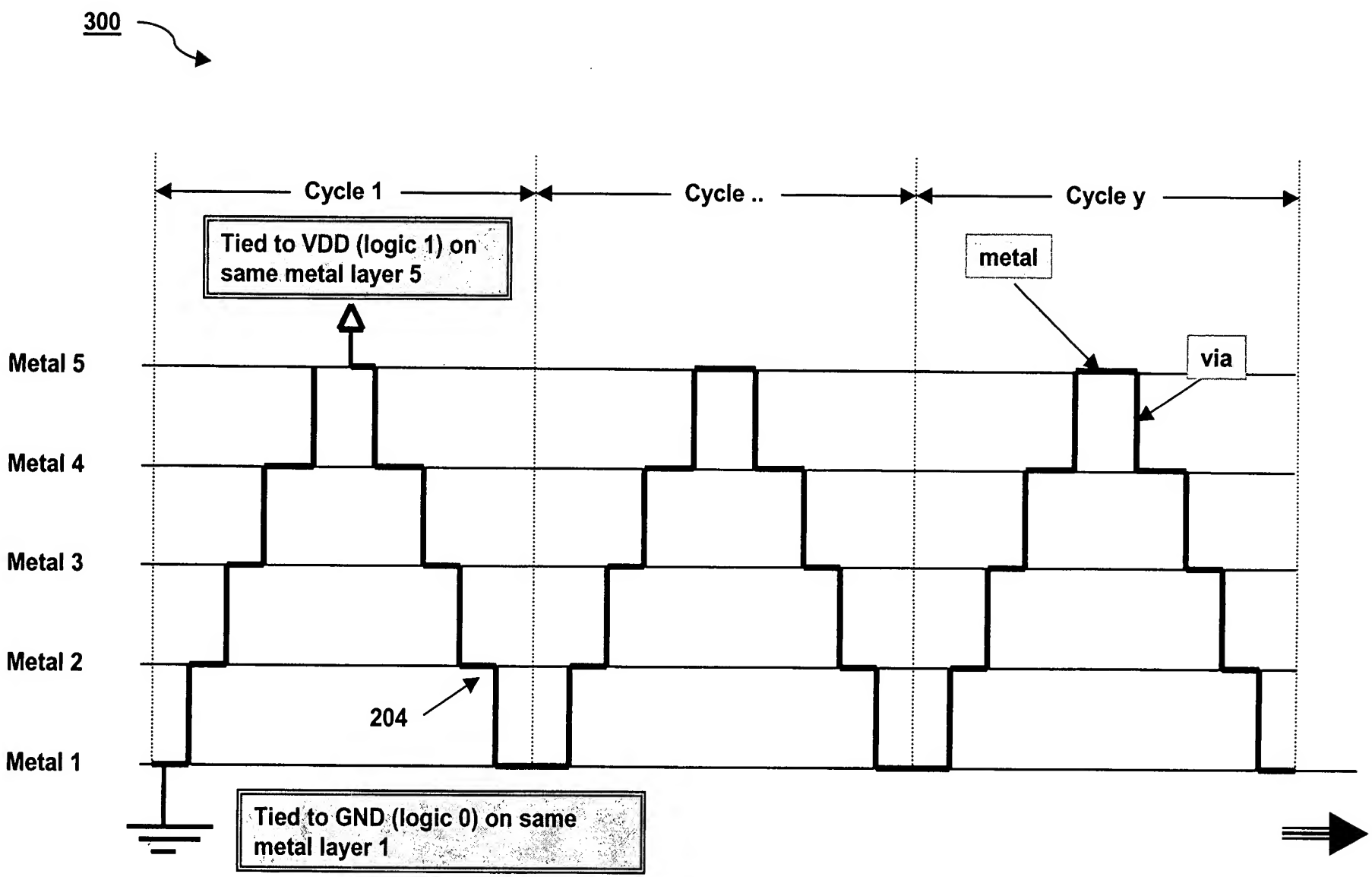

300
Cycle 1
Cycle ..
Cycle y
Tied to VDD (logic 1) on same metal layer 5
metal
via
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
204
Tied to GND (logic 0) on same metal layer 1
RevID<0> = 1

FIG. 3B

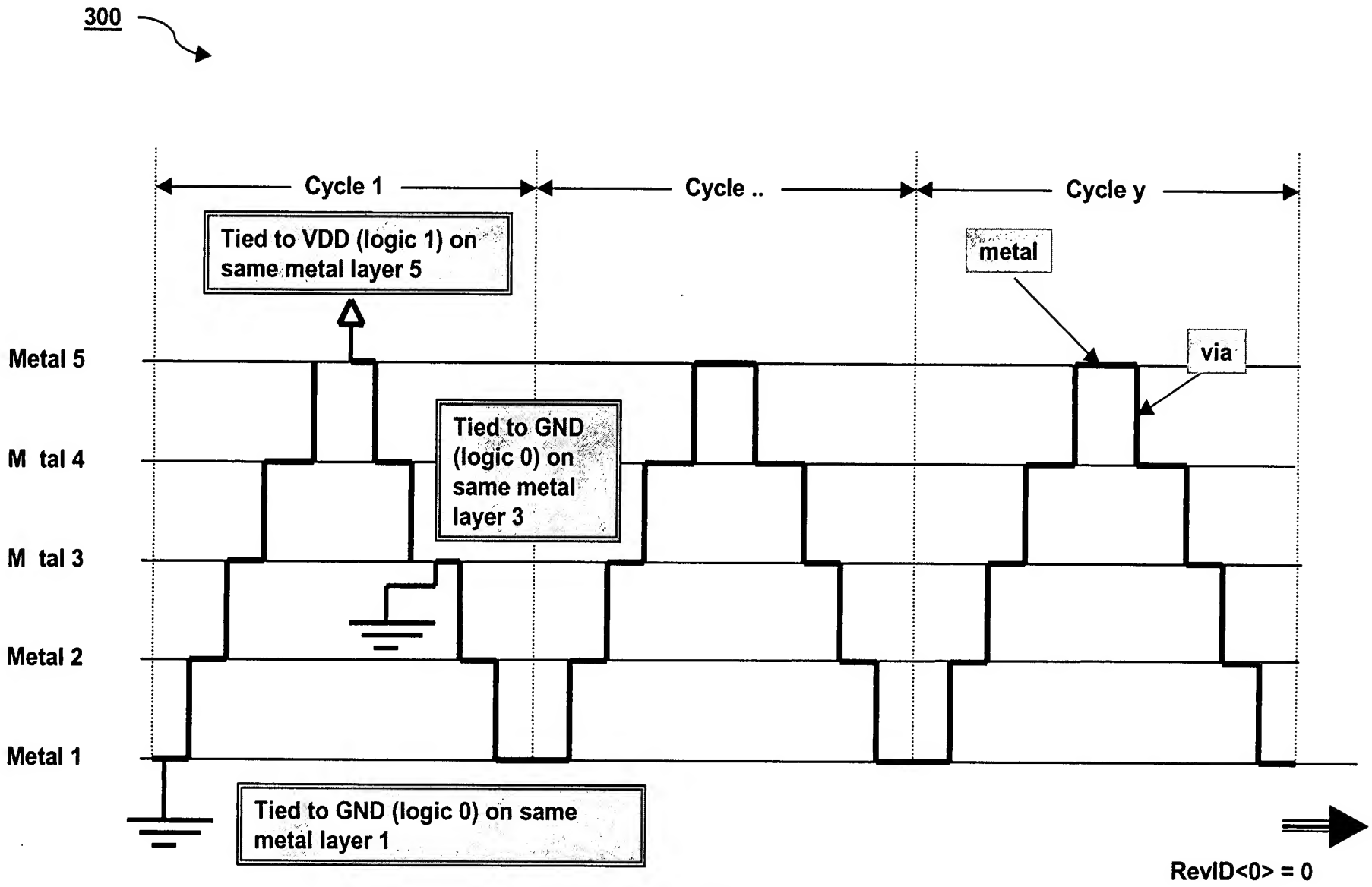

300
Cycle 1
Cycle ..
Cycle y
Tied to VDD (logic 1) on same metal layer 5
metal
via
Metal 5
M tal 4
M tal 3
Metal 2
Metal 1
Tied to GND (logic 0) on same metal layer 3
Tied to GND (logic 0) on same metal layer 1
RevID<0> = 0

FIG. 3C

400

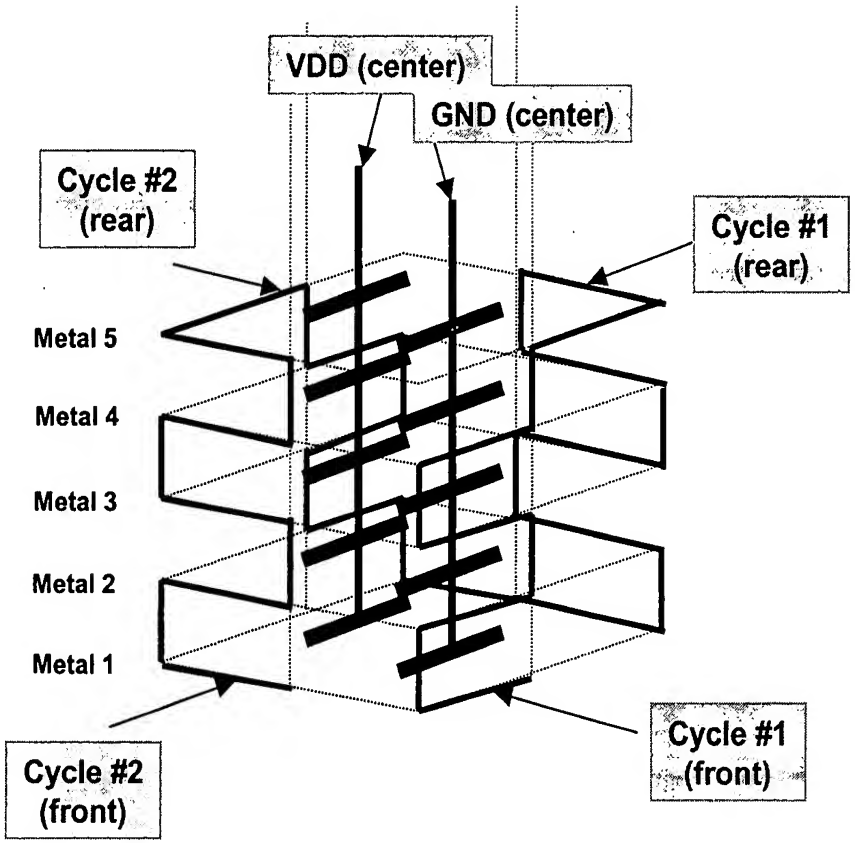

VDD (center)
GND (center)
Cycle #2 (rear)
Cycle #1 (rear)
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Cycle #2 (front)
Cycle #1 (front)

FIG. 4

500

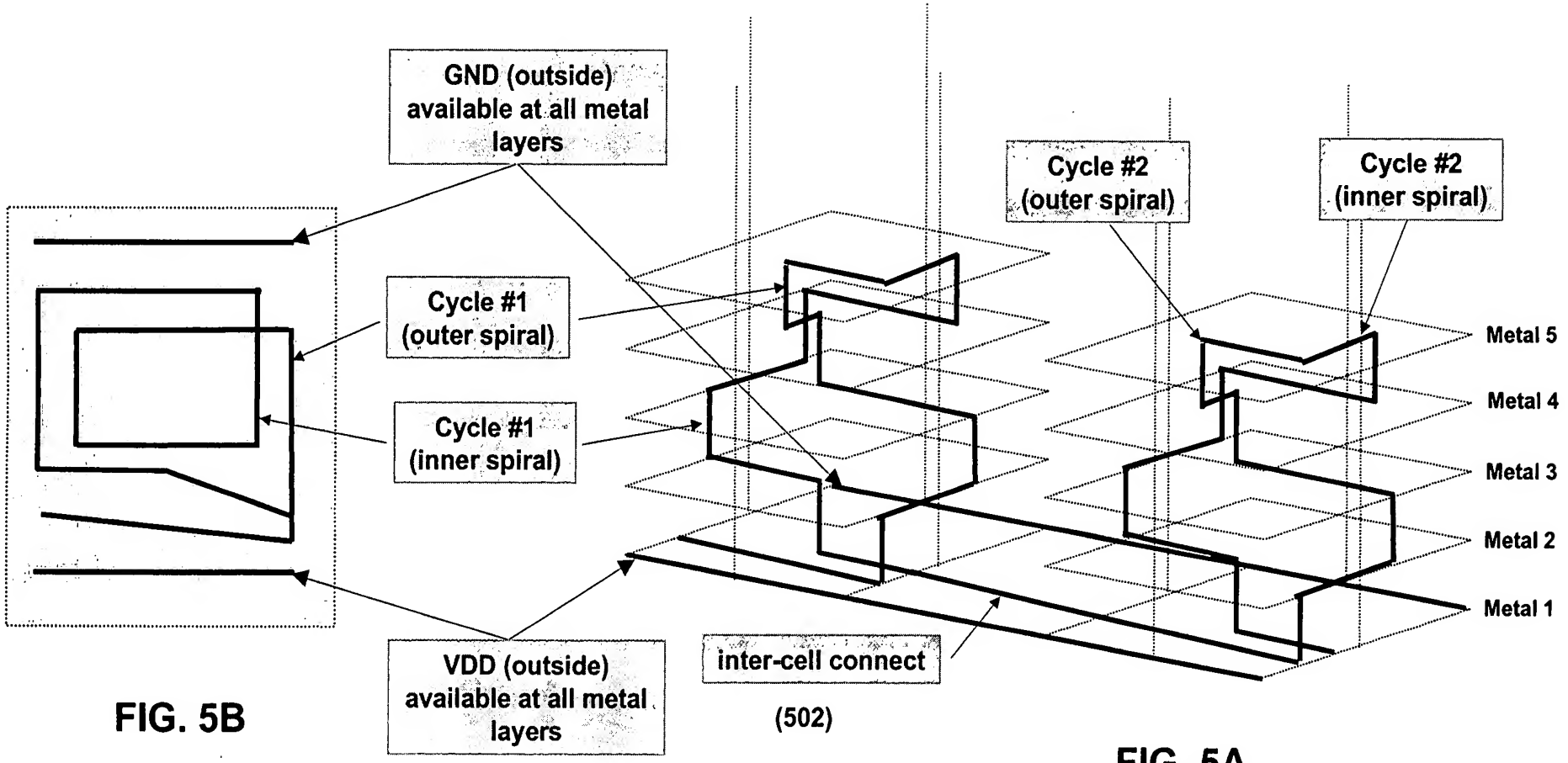


FIG. 5B

FIG. 5A

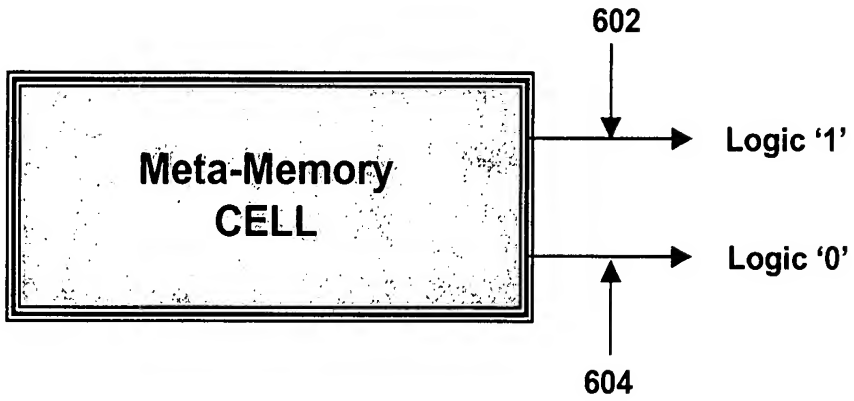


FIG. 6

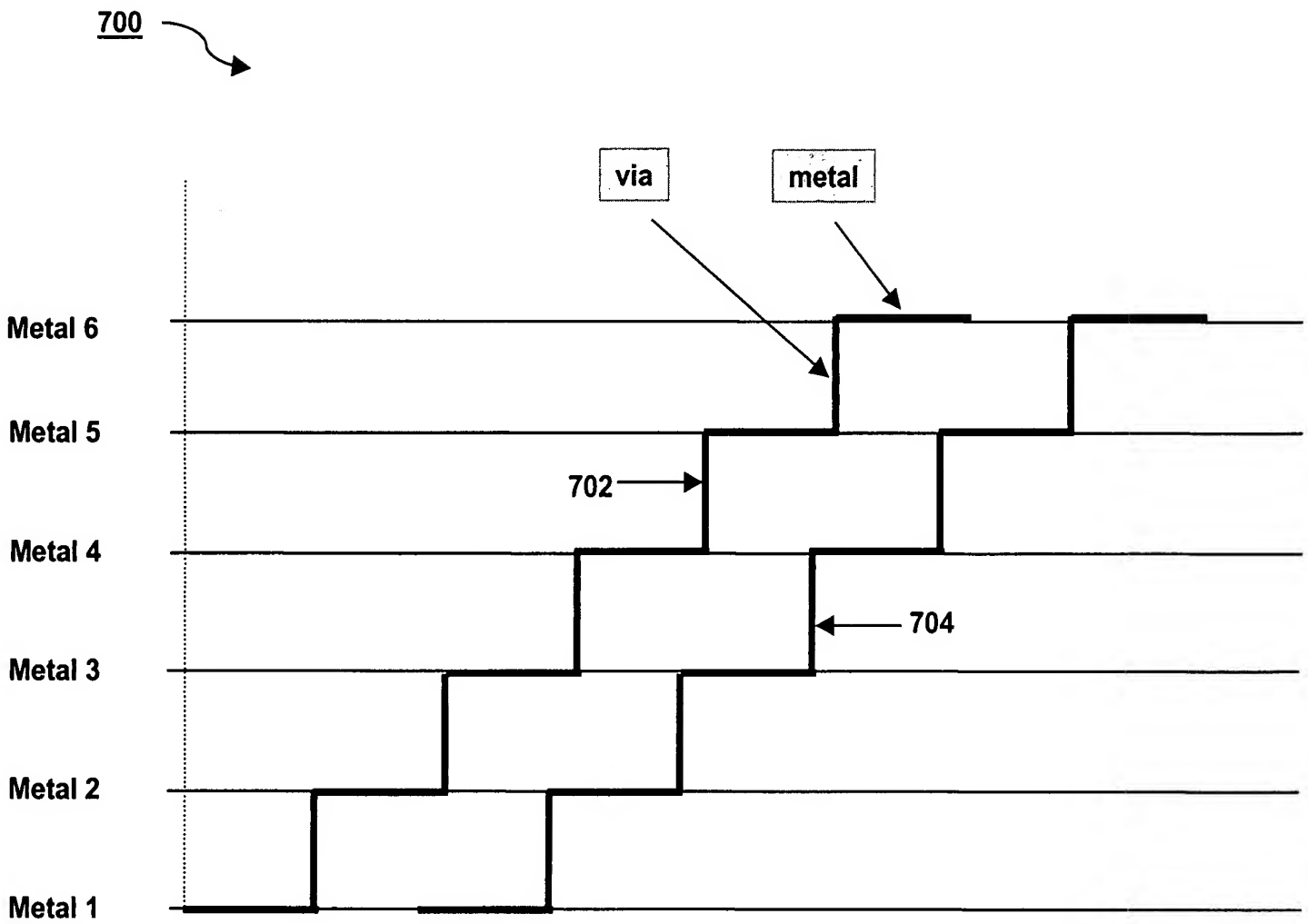

700
via
metal
Metal 6
Metal 5
702
Metal 4
704
Metal 3
Metal 2
Metal 1

FIG. 7A

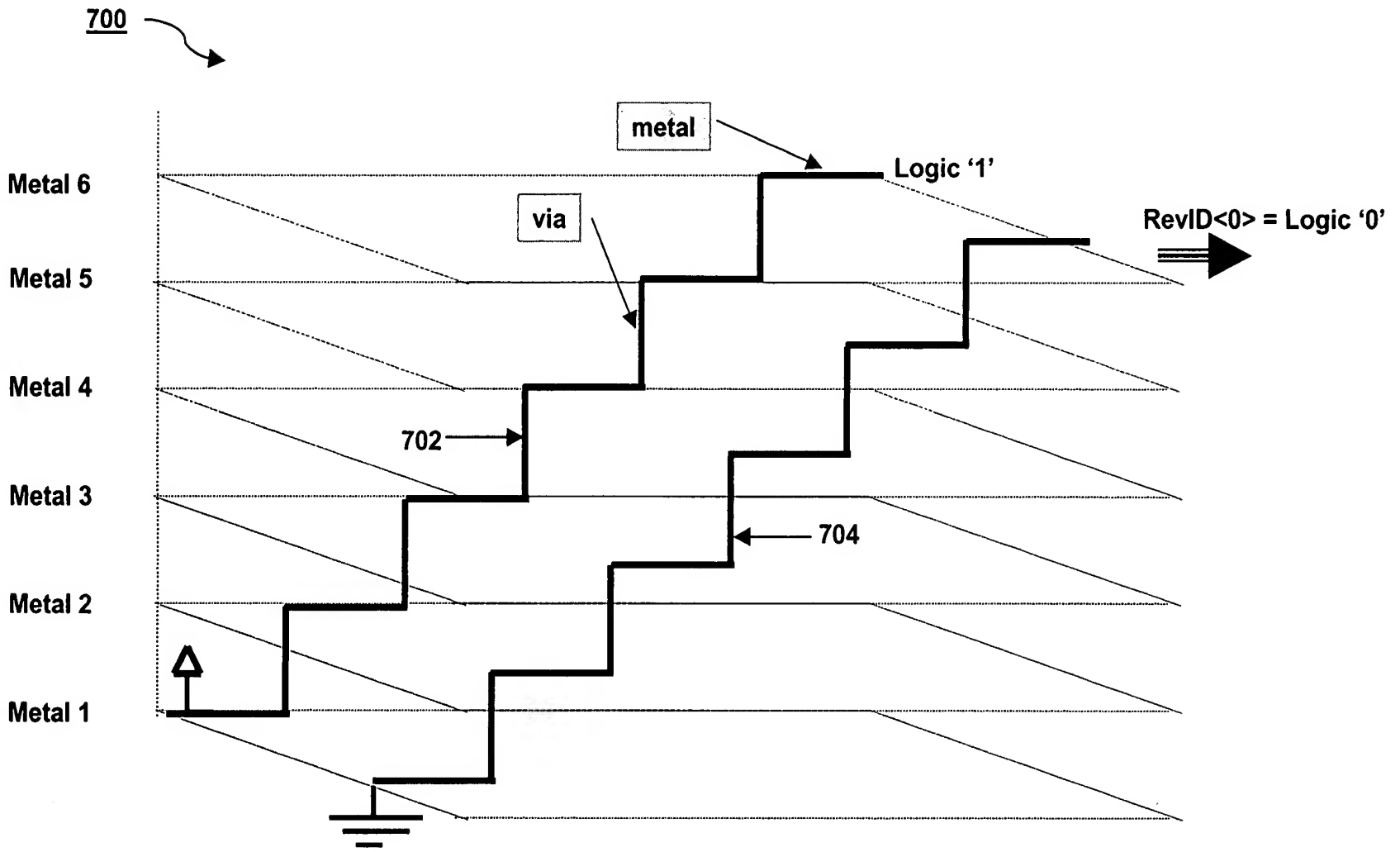

700
metal
Logic '1'
via
RevID<0> = Logic '0'
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
702
704

FIG. 7B

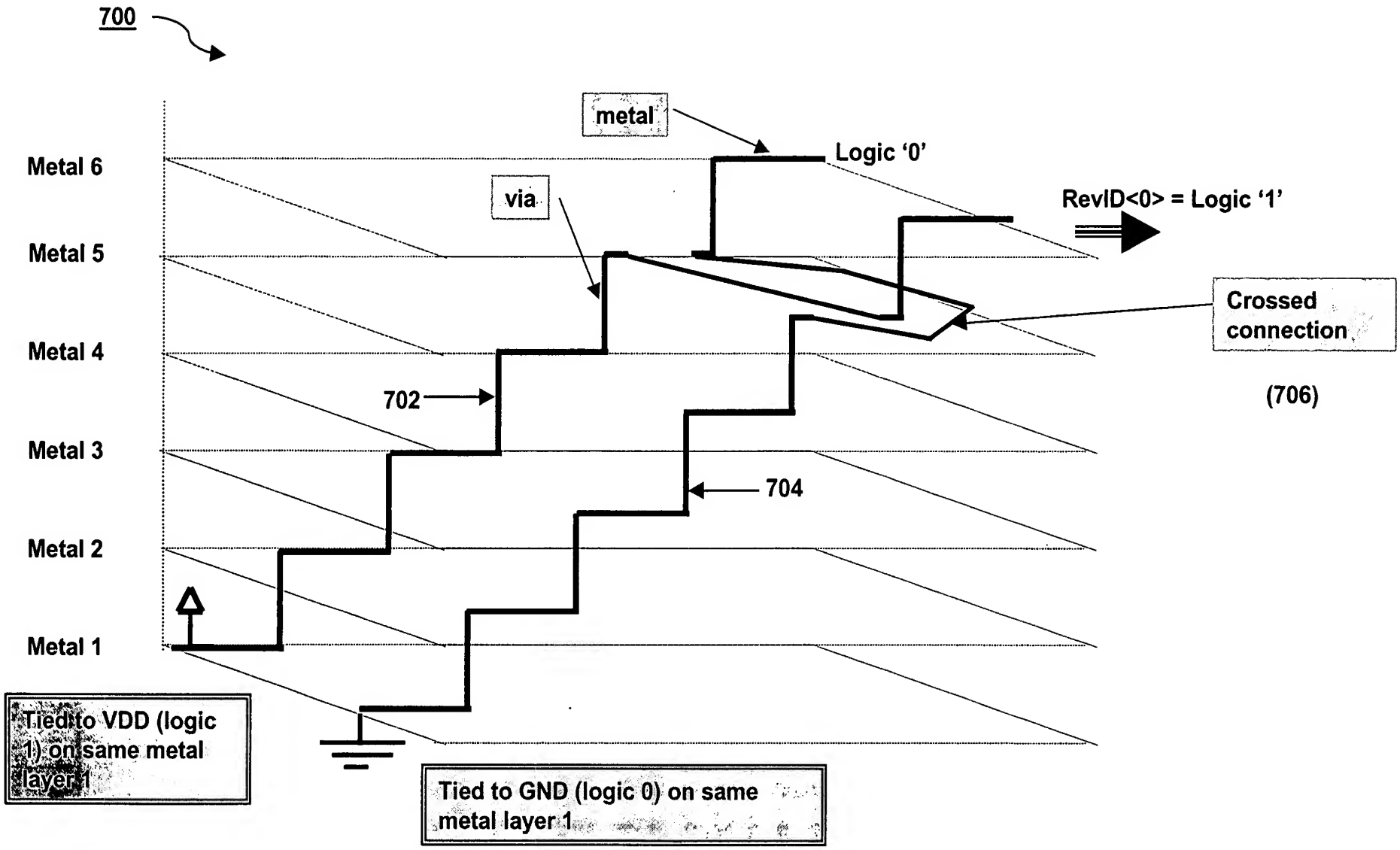

700
metal
Logic '0'
via
RevID<0> = Logic '1'
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Crossed connection
(706)
702
704
Tied to VDD (logic 1) on same metal layer 1
Tied to GND (logic 0) on same metal layer 1

FIG. 7C

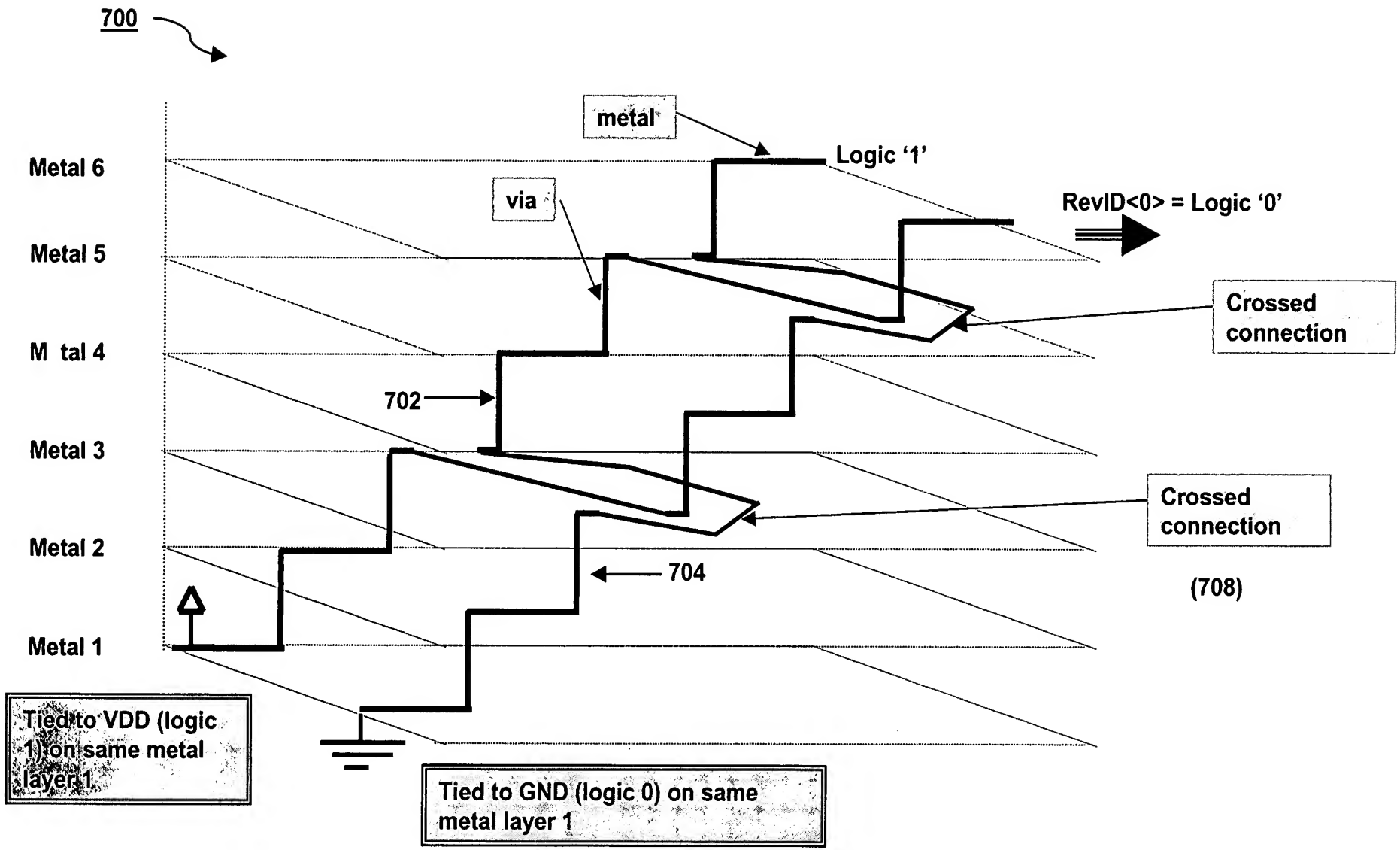

700
metal
Logic '1'
via
RevID<0> = Logic '0'
Metal 6
Metal 5
M tal 4
Metal 3
Metal 2
Metal 1
Crossed connection
Crossed connection
702
704
(708)
Tied to VDD (logic 1) on same metal layer 1
Tied to GND (logic 0) on same metal layer 1

FIG. 7D

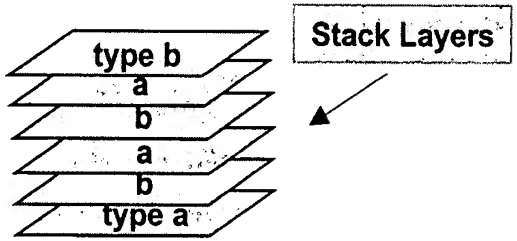

Stack Layers
type b
a
b
a
b
type a

FIG. 8A

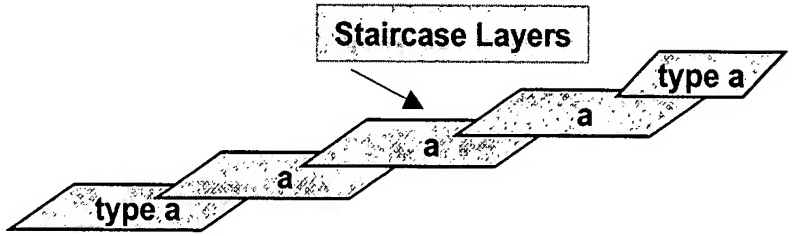

Staircase Layers
type a
a
a
a
type a

FIG. 8B


A_in
B_in
Metal/Via Layer
A_out
B_out

FIG. 9A

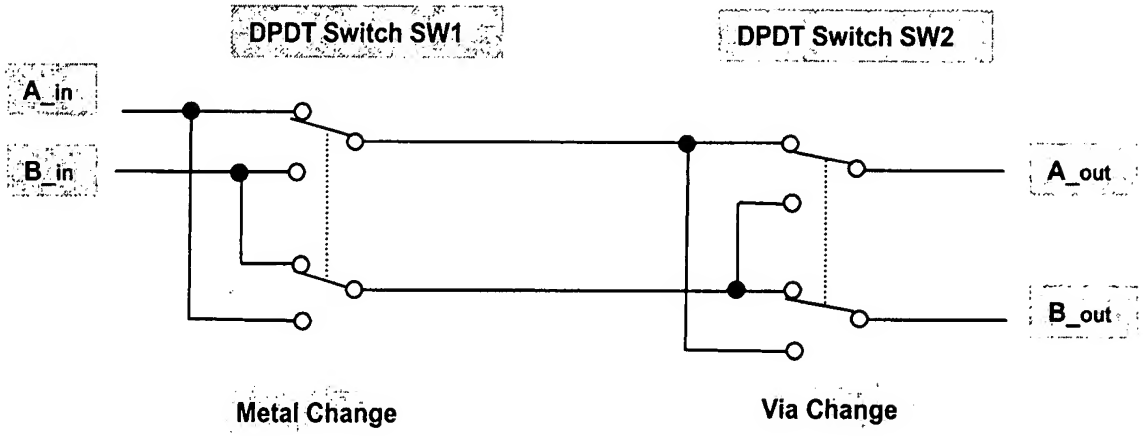

DPDT Switch SW1
DPDT Switch SW2
A_in
B_in
A_out
B_out
Metal Change
Via Change

FIG. 9B

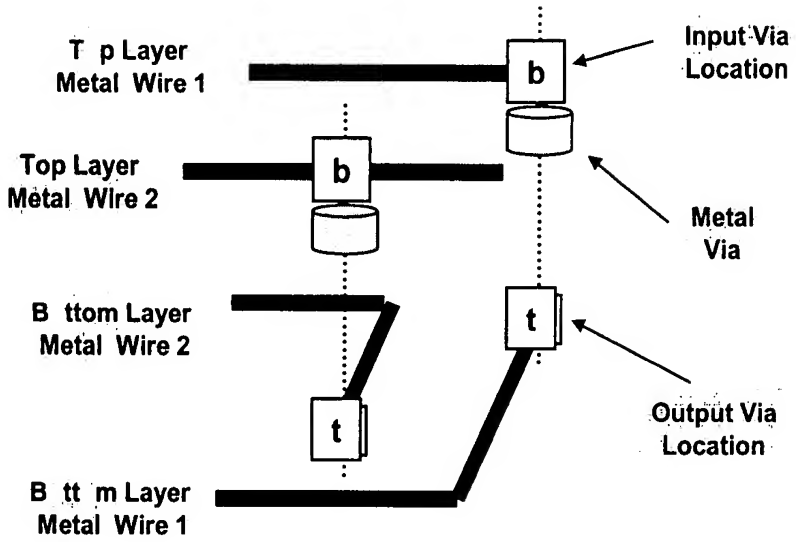
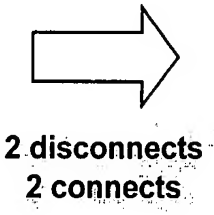

T p Layer
Metal Wire 1
Top Layer
Metal Wire 2
B ttom Layer
Metal Wire 2
B tt m Layer
Metal Wire 1
b
b
t
t
Input Via
Location
Metal
Via
Output Via
Location

FIG. 9C


2 disconnects
2 connects

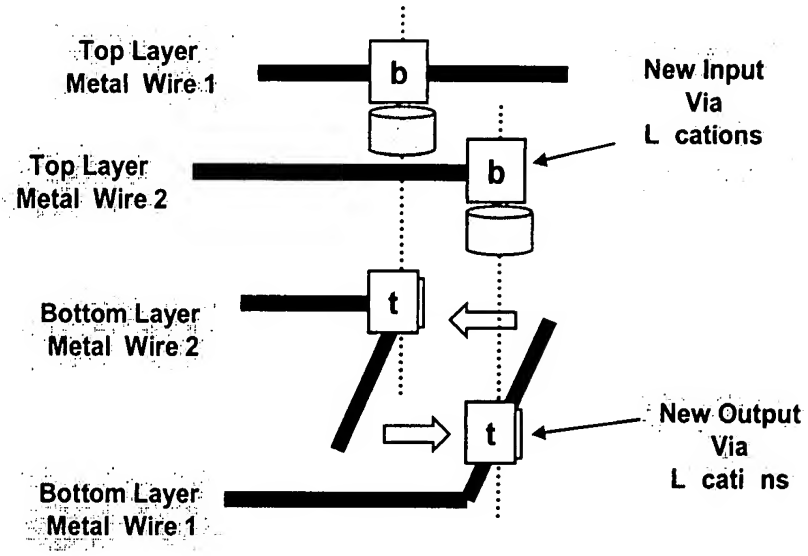

Top Layer
Metal Wire 1
Top Layer
Metal Wire 2
Bottom Layer
Metal Wire 2
Bottom Layer
Metal Wire 1
b
b
t
t
New Input
Via
L cations
New Output
Via
L cati ns

FIG. 9D

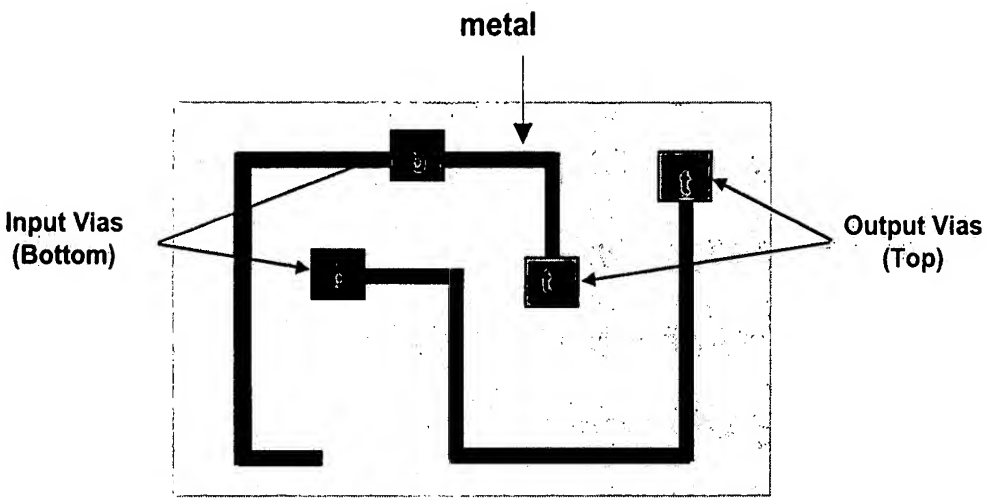


FIG. 10A

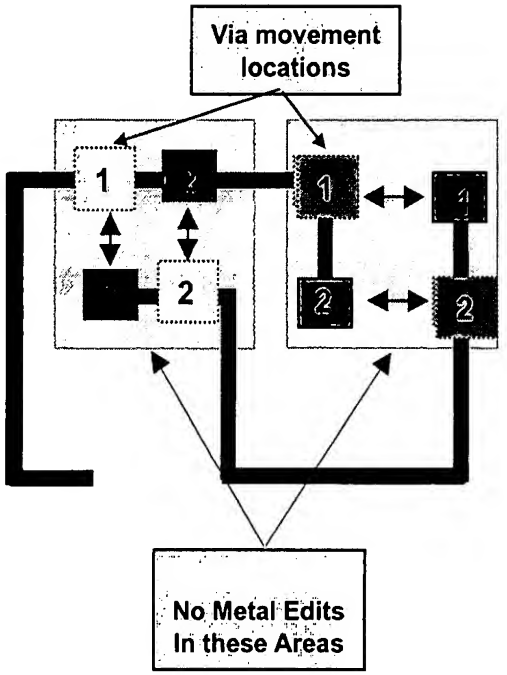
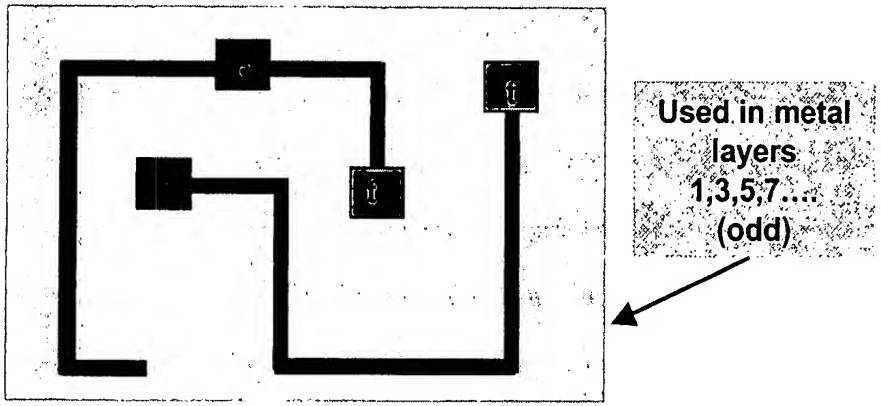


FIG. 10B

FIG. 11A



Basic Pattern

Basic Pattern w/ Metal Change (2 cuts, 2 jumps)

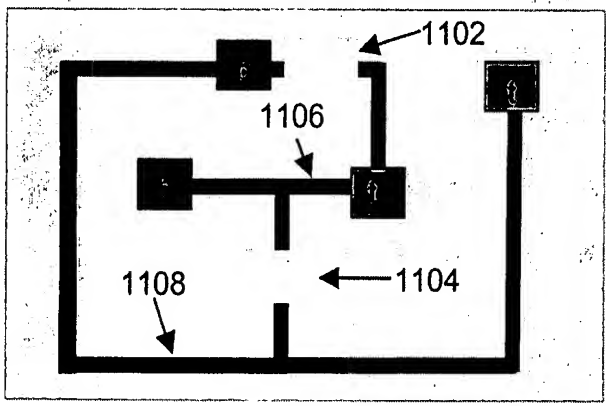
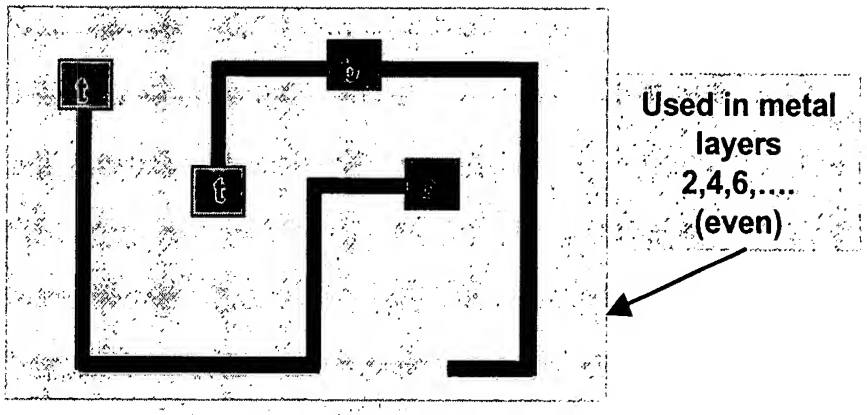


FIG. 11B

FIG. 11C



Flip Basic Pattern

Flip Basic Pattern w/ Metal Change (2 cuts, 2 jumps)

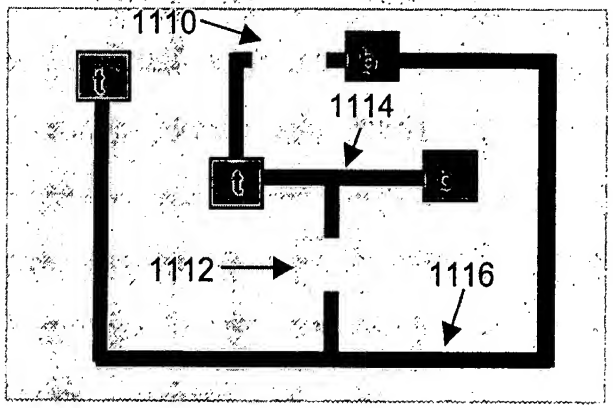
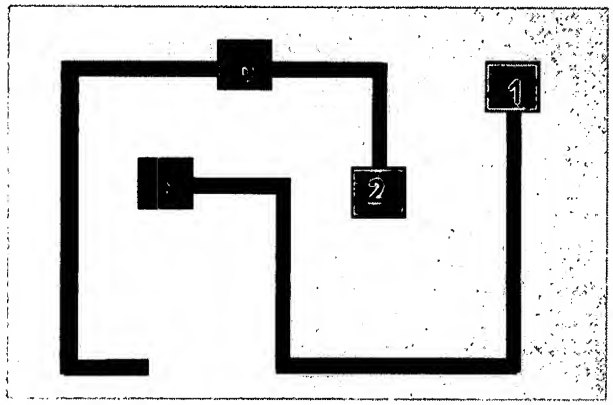


FIG. 11D

FIG. 12A



Basic Pattern

Basic Pattern w/ Via Change
(2 disconnects, 2 connects)

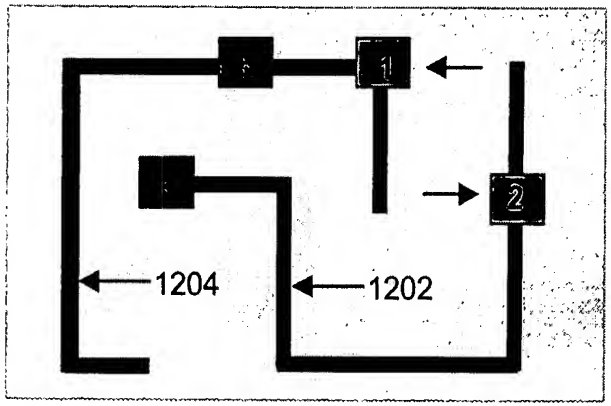
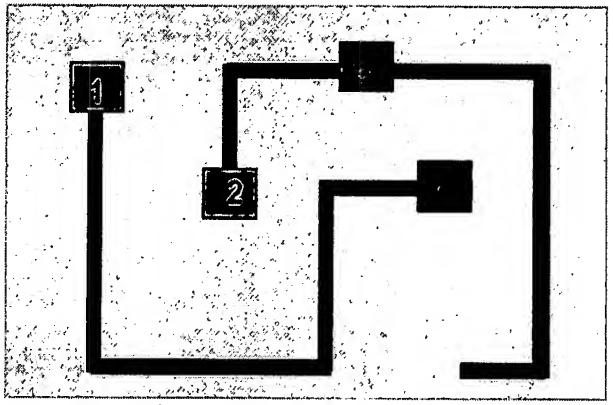


FIG. 12B

FIG. 12C



Flip Basic Pattern

Flip Basic Pattern w/ Via Change
(2 disconnects, 2 connects)

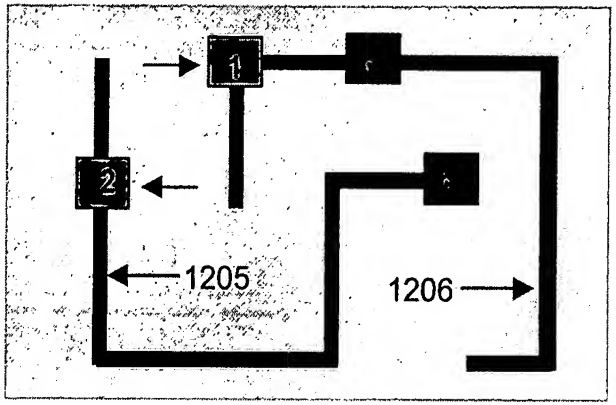


FIG. 12D

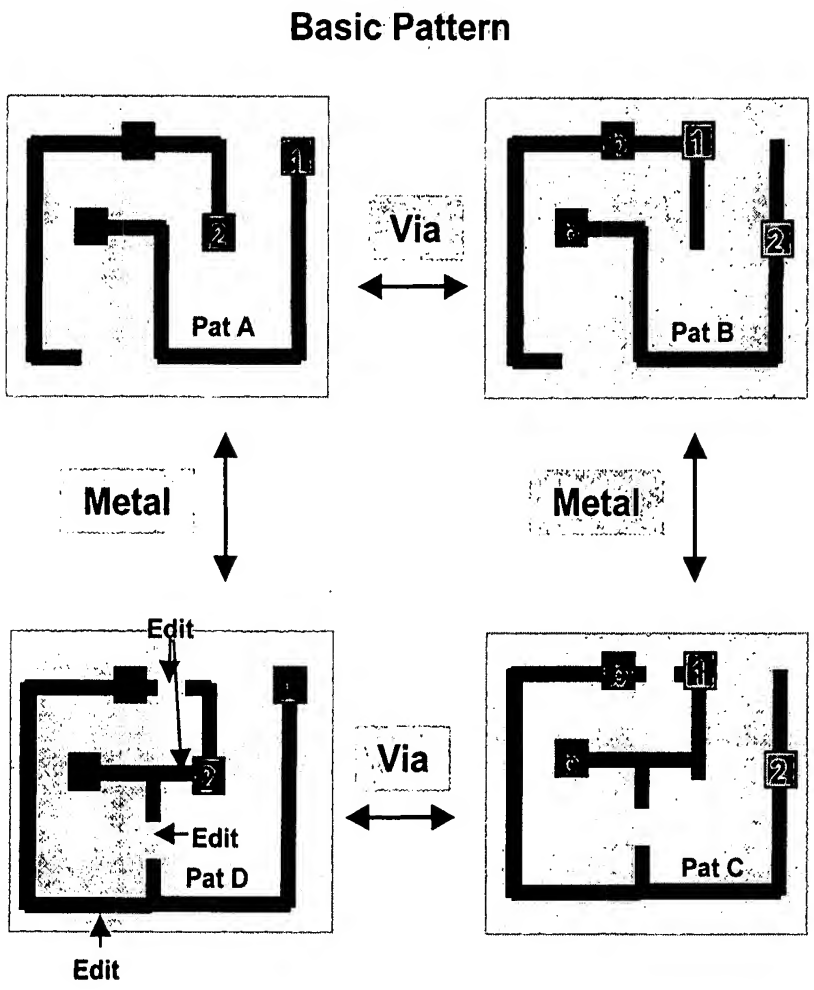

Basic Pattern
Pat A
Via
Pat B
Metal
Metal
Edit
Edit
Pat D
Via
Pat C
Edit

FIG. 13

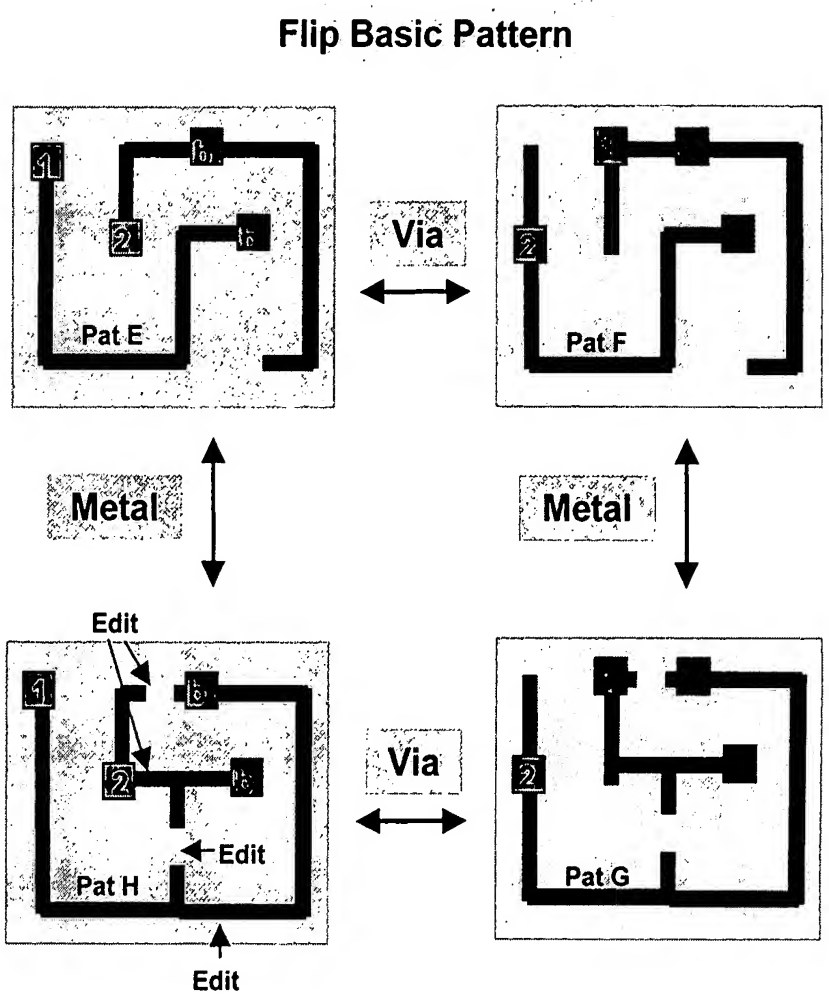

Flip Basic Pattern
Pat E
Via
Pat F
Metal
Metal
Edit
Edit
Pat H
Via
Pat G
Edit

FIG. 14

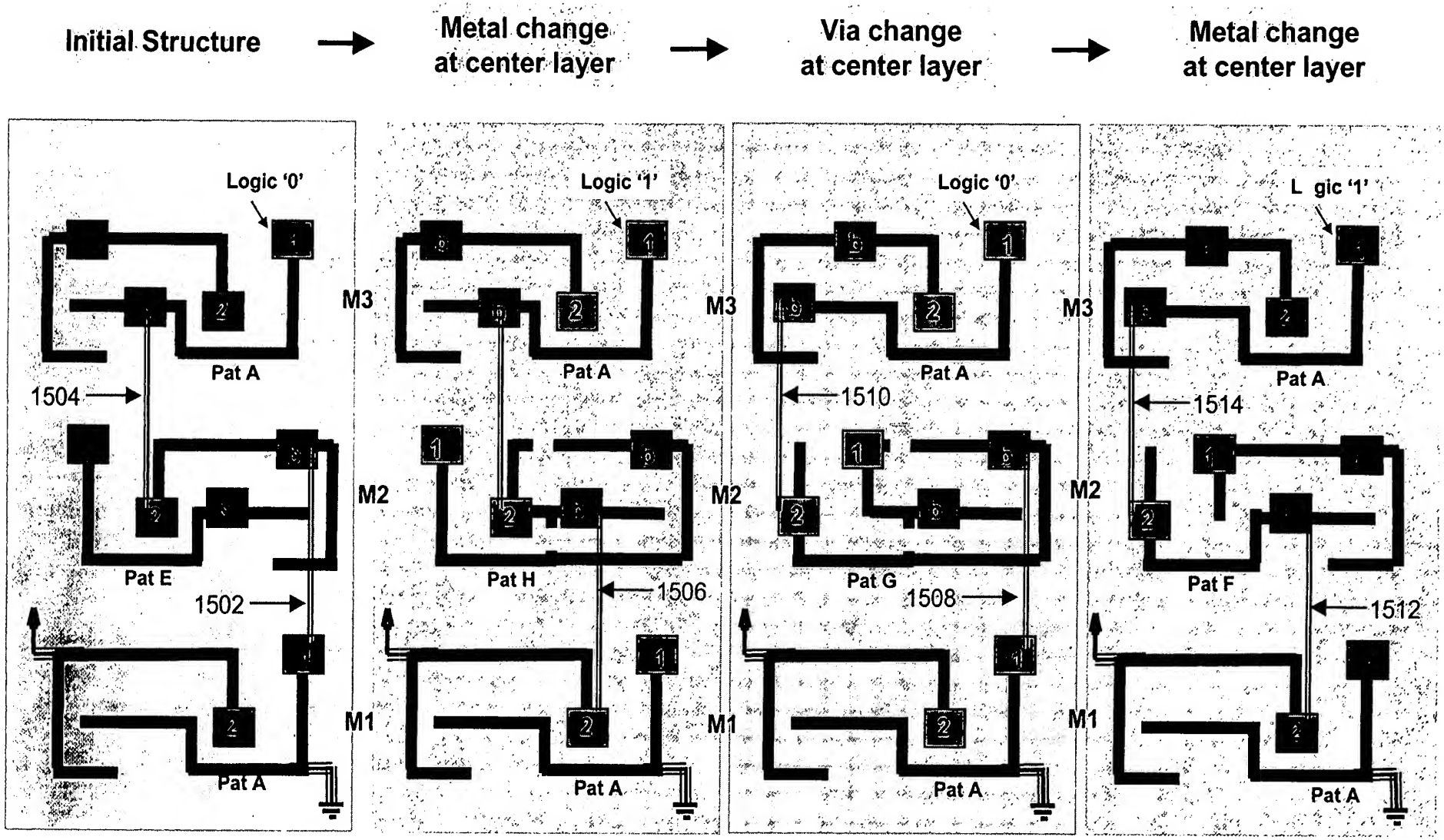


FIG. 15A FIG. 15B FIG. 15C FIG. 15D

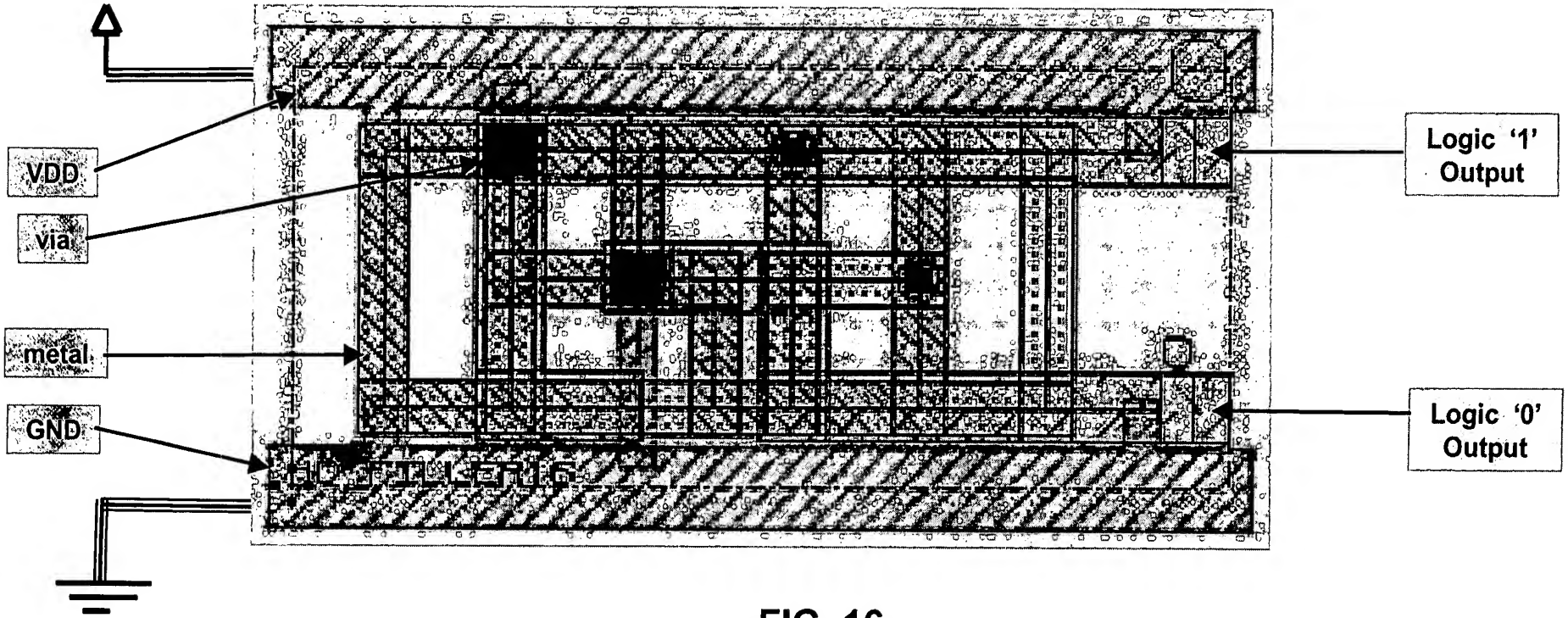
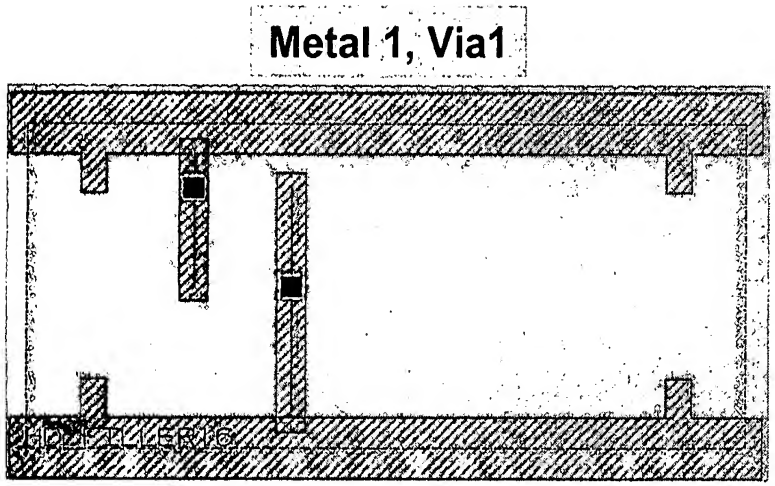
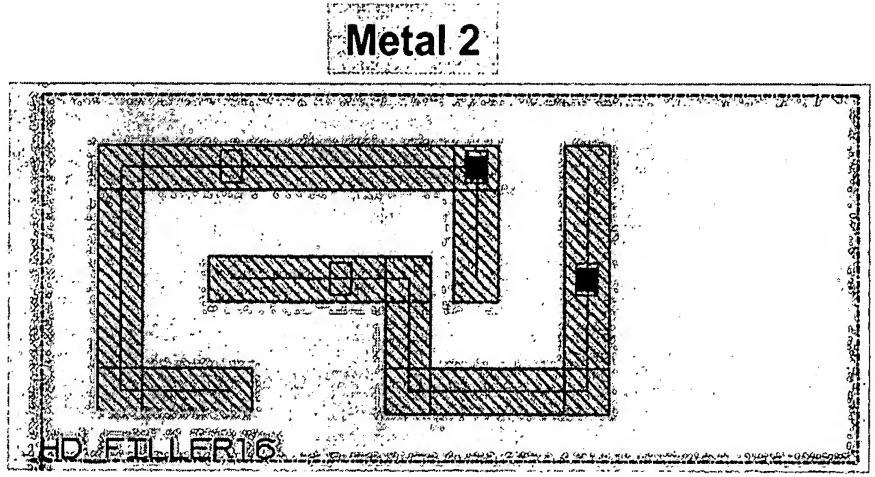


FIG. 16

FIG. 17A

FIG. 17B





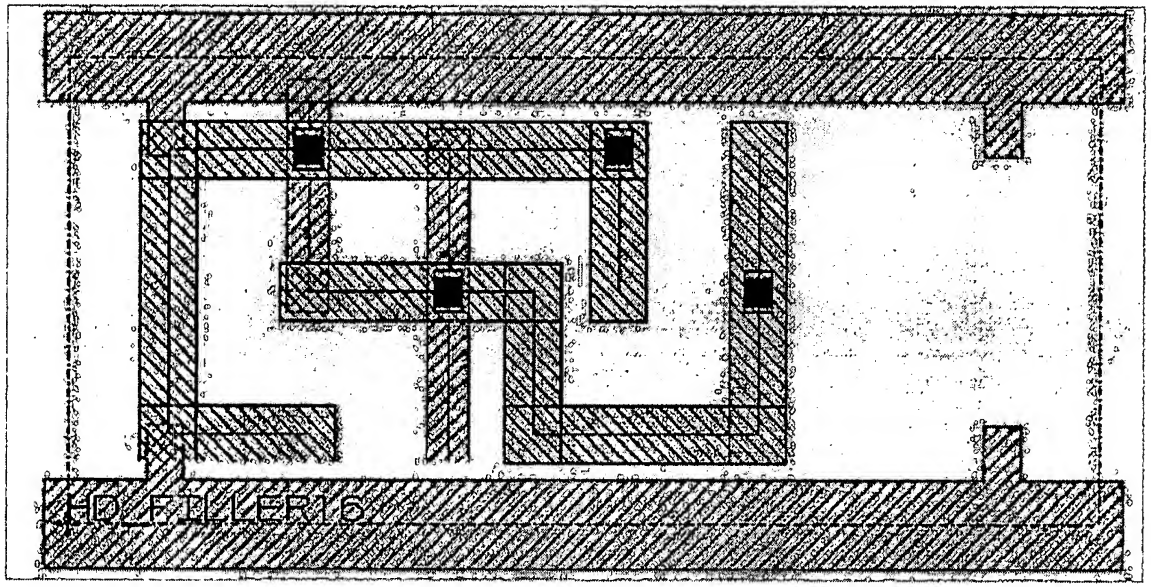


FIG. 17C

FIG. 18A

FIG. 18B

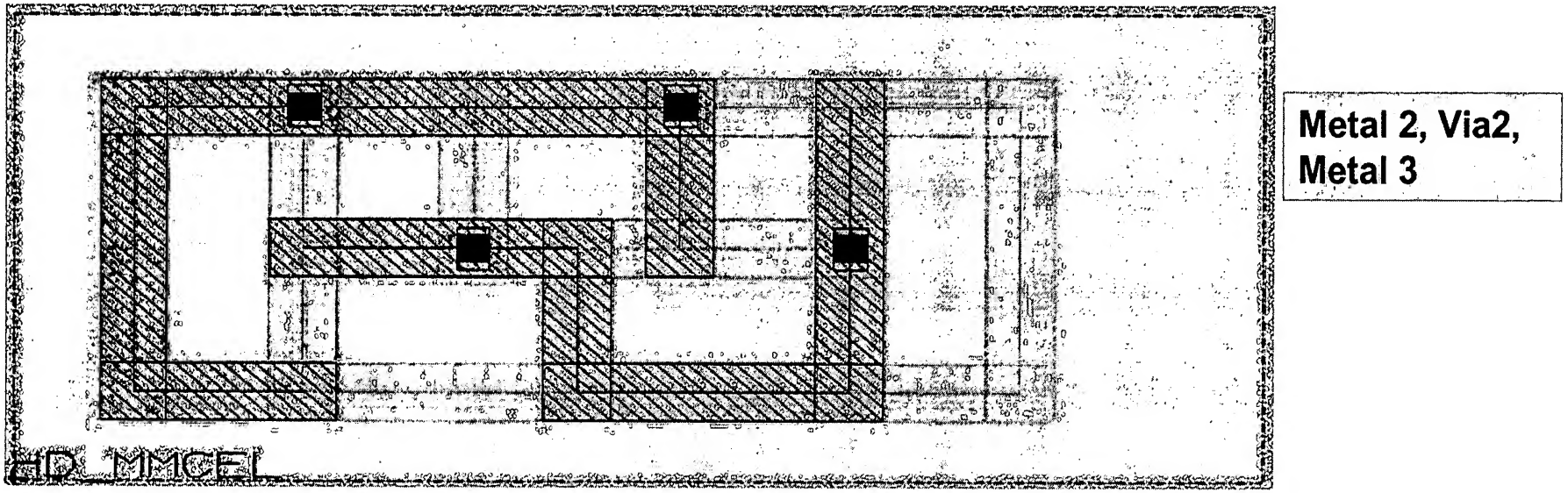


FIG. 18C

FIG. 19A

Metal 3, Via3

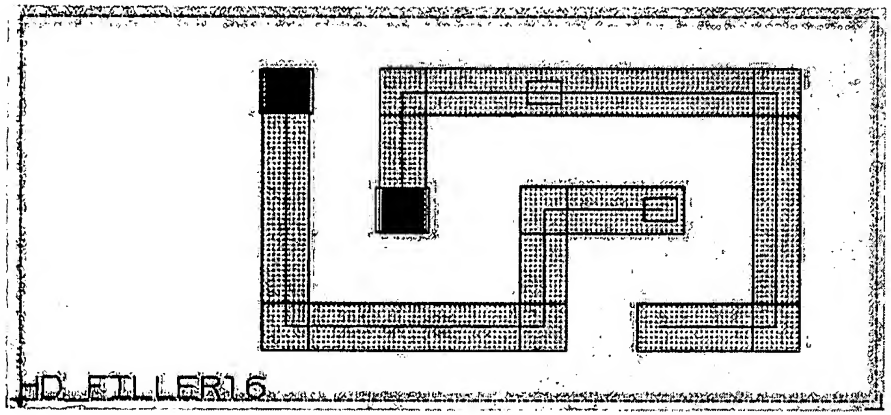
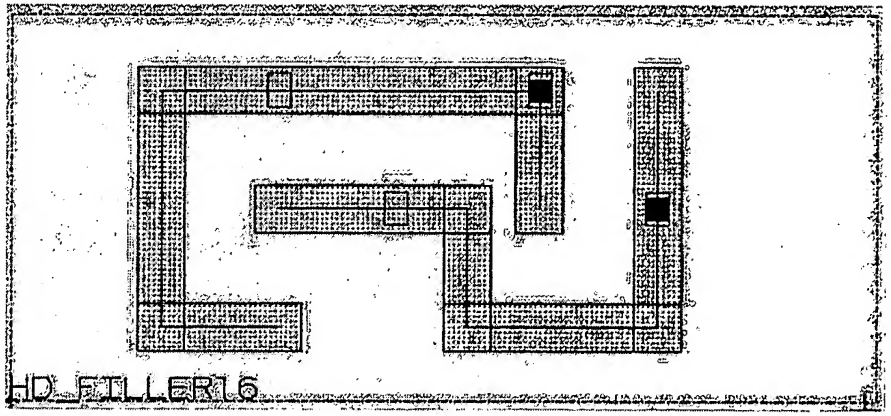
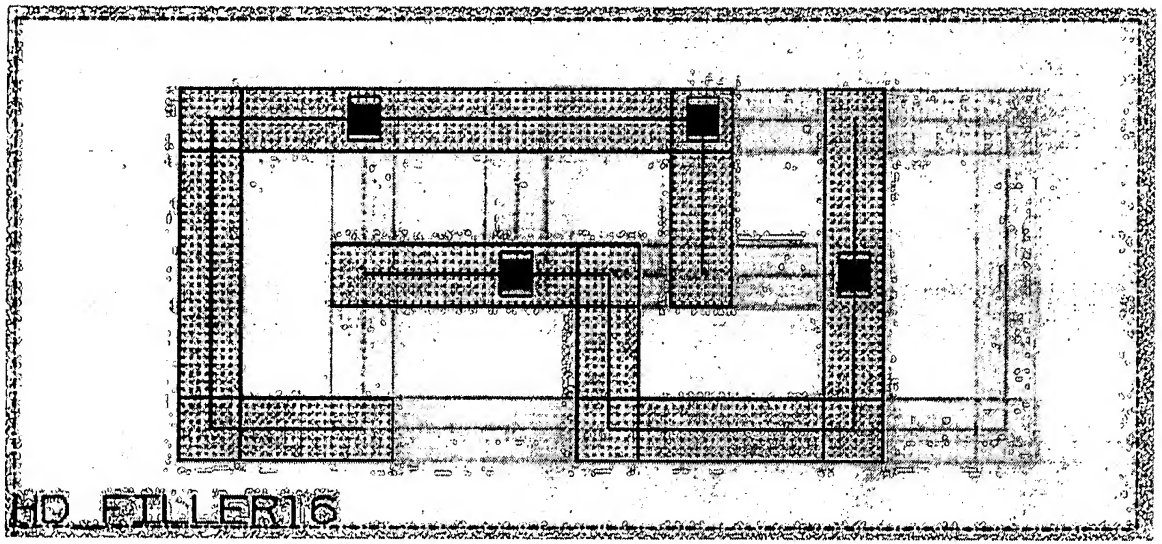


FIG. 19B

Metal 4





Metal 3, Via3,
Metal 4

FIG. 19C

FIG. 20A

Metal 4, Via4

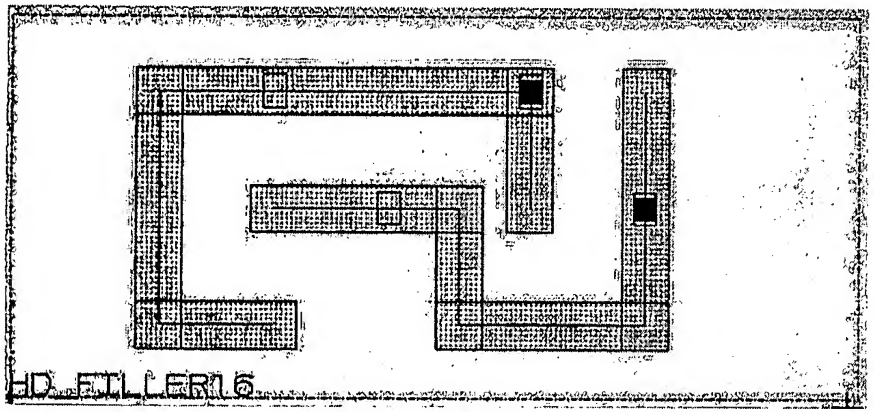
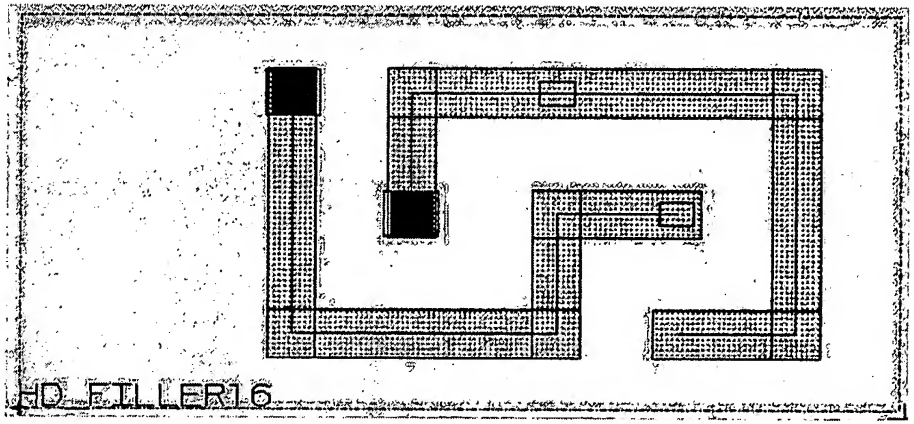
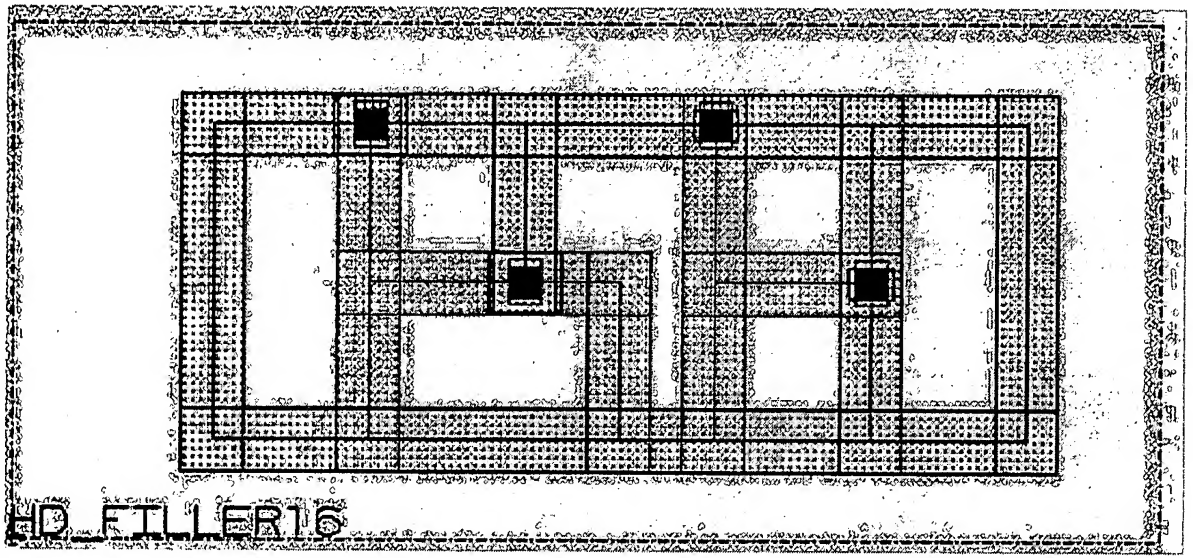


FIG. 20B

Metal 5





Metal 4, Via4, Metal 5

FIG. 20C

FIG. 21A

Metal 5, Via5

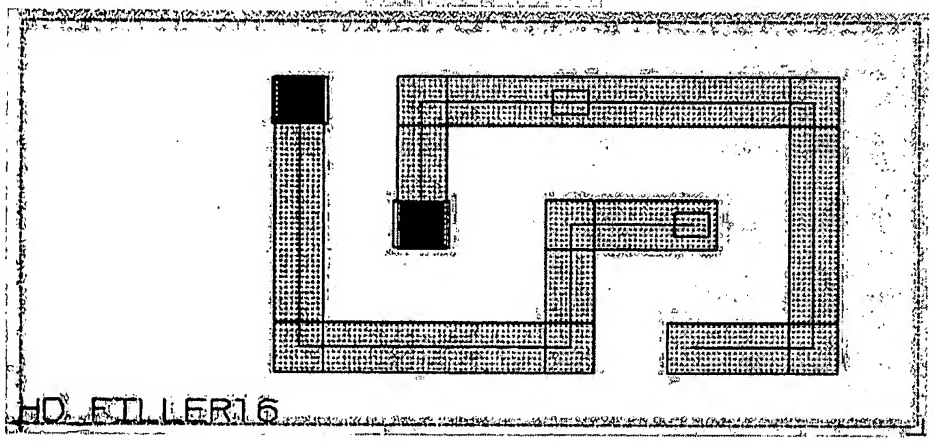
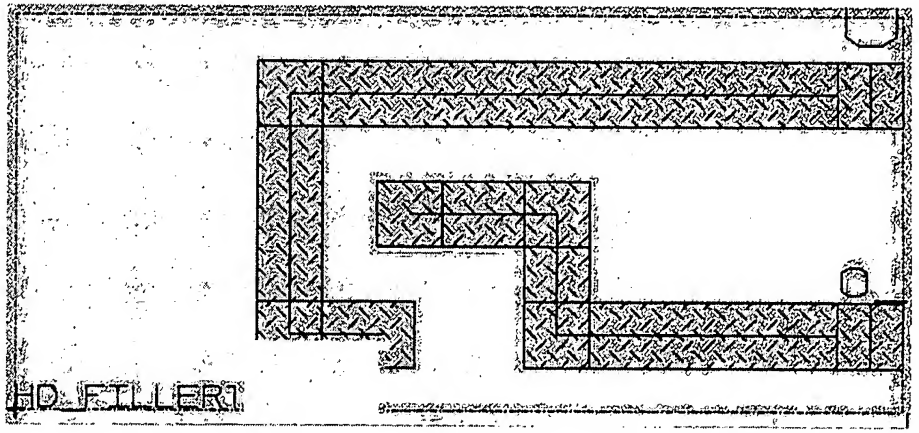
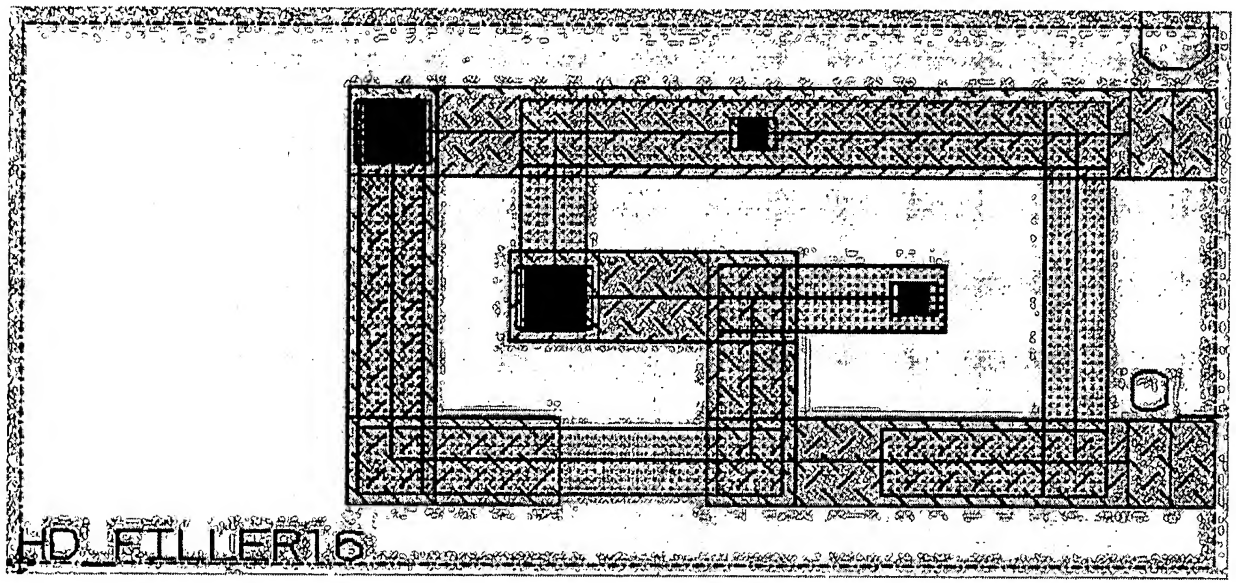


FIG. 21B

Metal 6





Metal 5, Via5, Metal 6

FIG. 21C

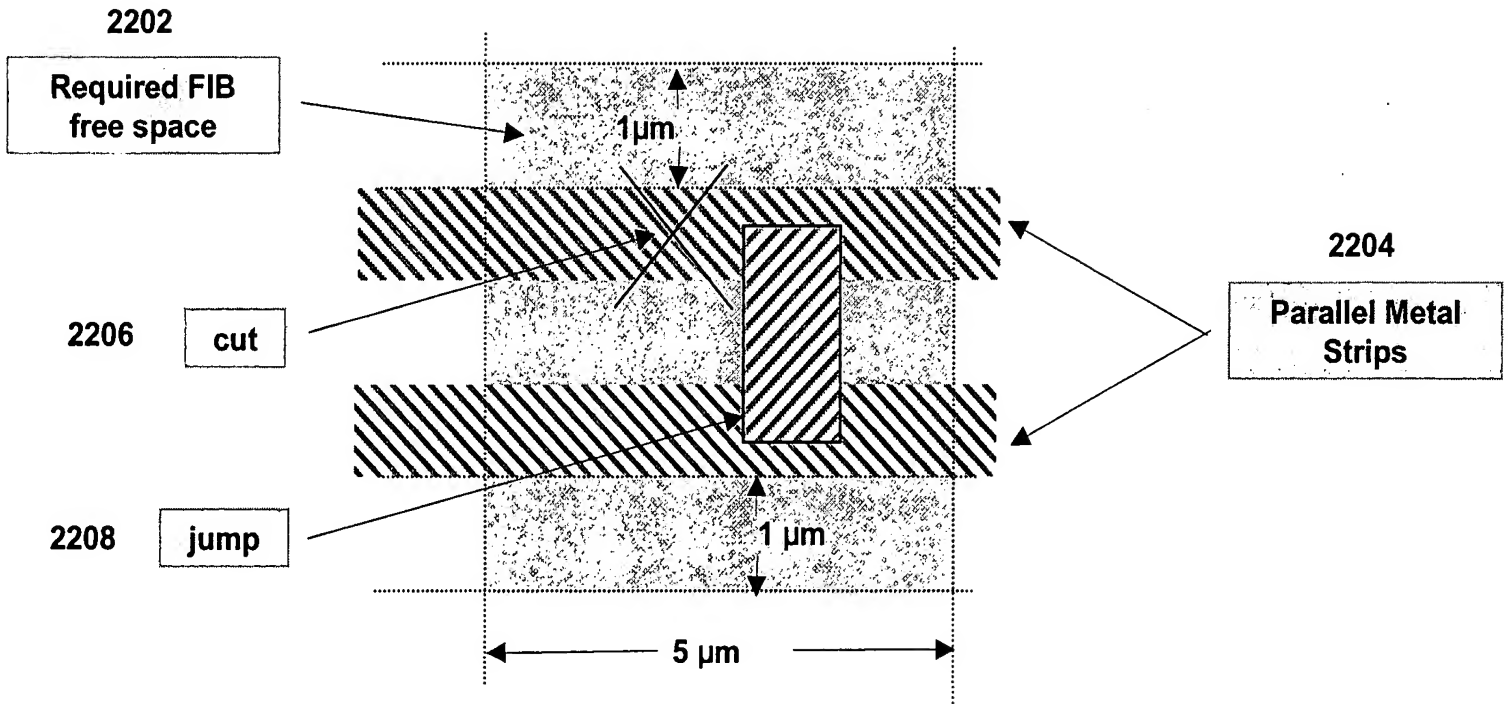

2202
Required FIB free space
1µm
2204
Parallel Metal Strips
2206
cut
2208
jump
1 µm
5 µm

FIG. 22

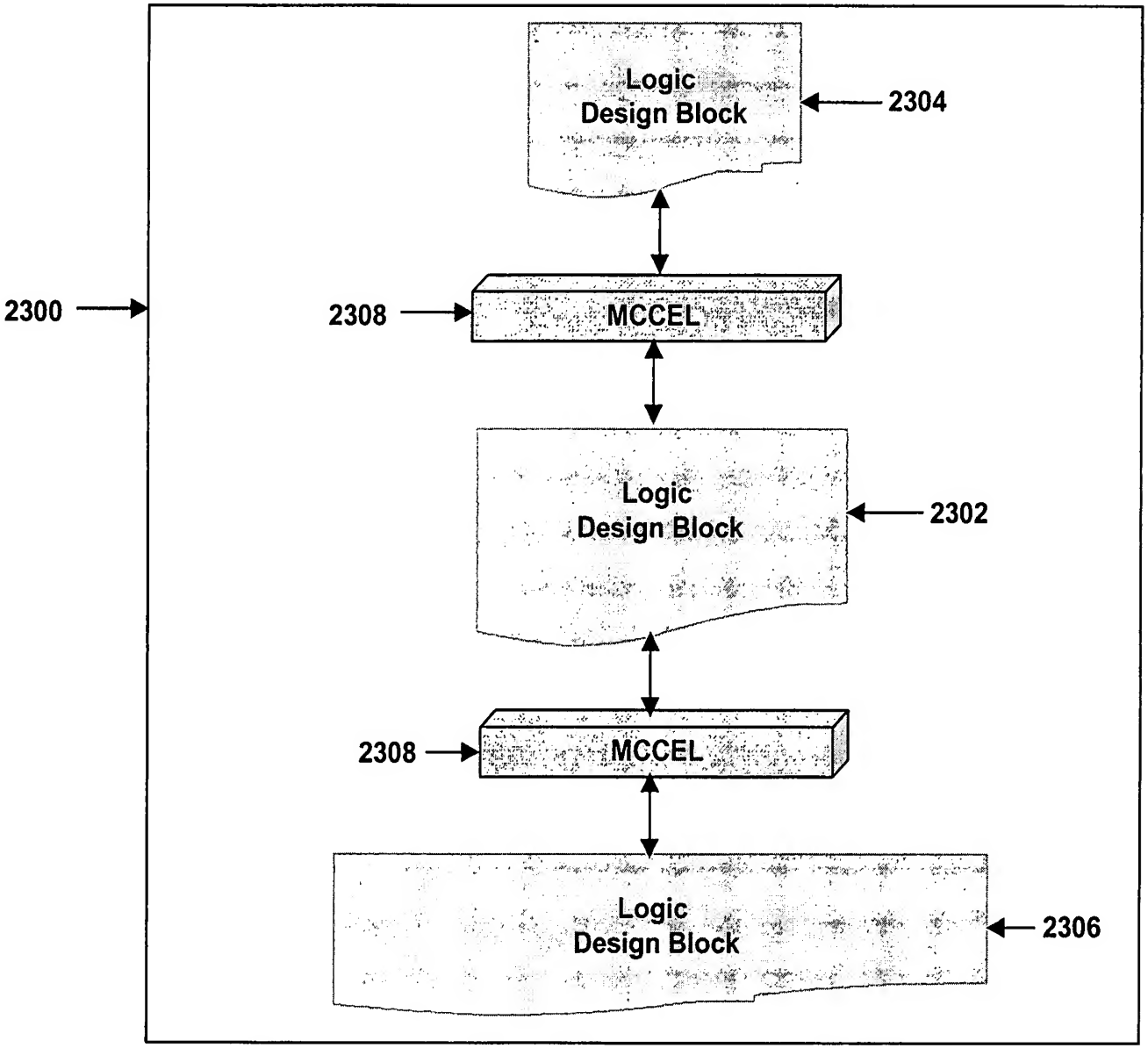

Logic
Design Block
2304
2300
2308
MCCEL
Logic
Design Block
2302
2308
MCCEL
Logic
Design Block
2306

FIG. 23

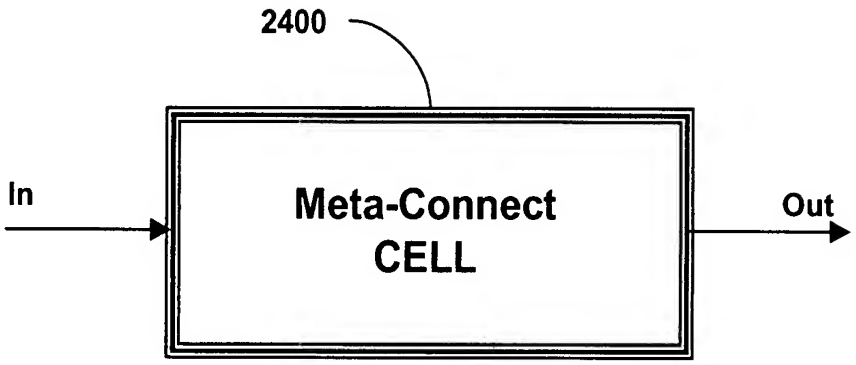


FIG. 24A

Out	Comment
In	Default Connect at any layer
0	Tied to GND at any layer
1	Tied to VDD at any layer

FIG. 24B

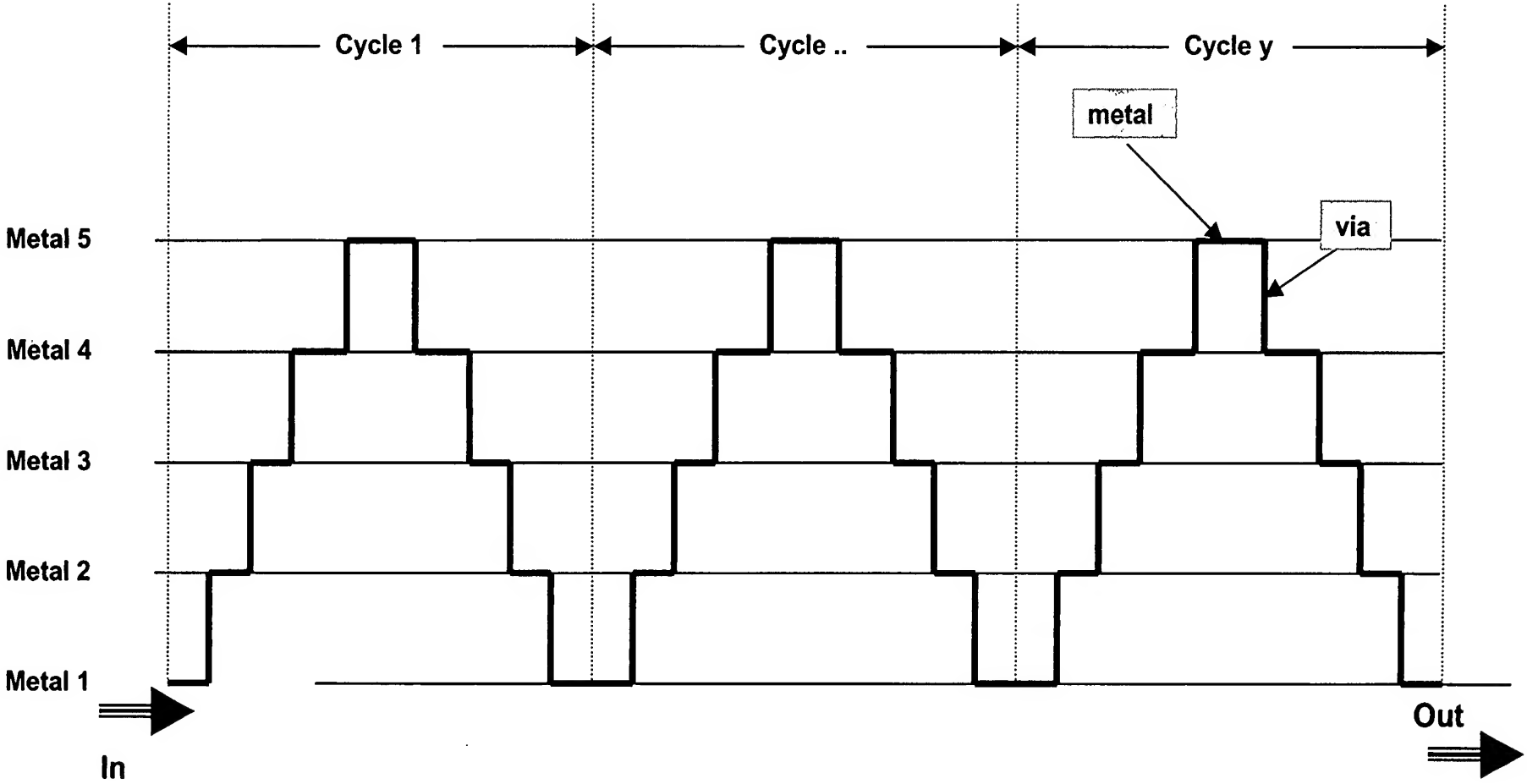

Cycle 1
Cycle ..
Cycle y
metal
via
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
In
Out

FIG. 25

FIG. 26A

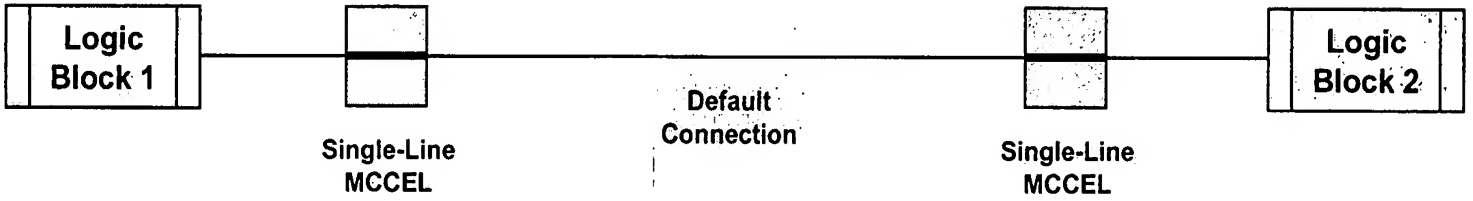


FIG. 26B

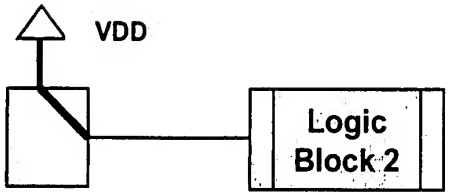
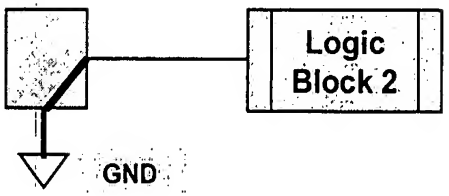


FIG. 26C



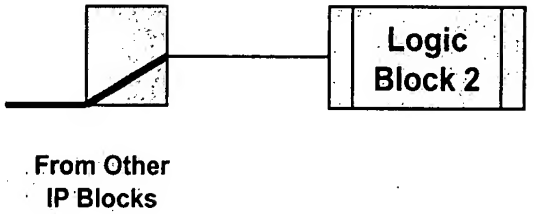


FIG. 26D

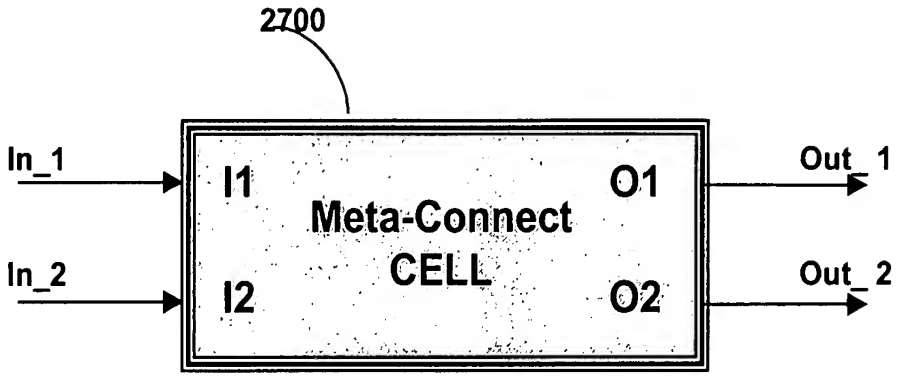


FIG. 27A

Toggle	Out_1	Out_2	Comment
0	In_1	In_2	Default
1	In_2	In_1	Metal/Via Change

FIG. 27B

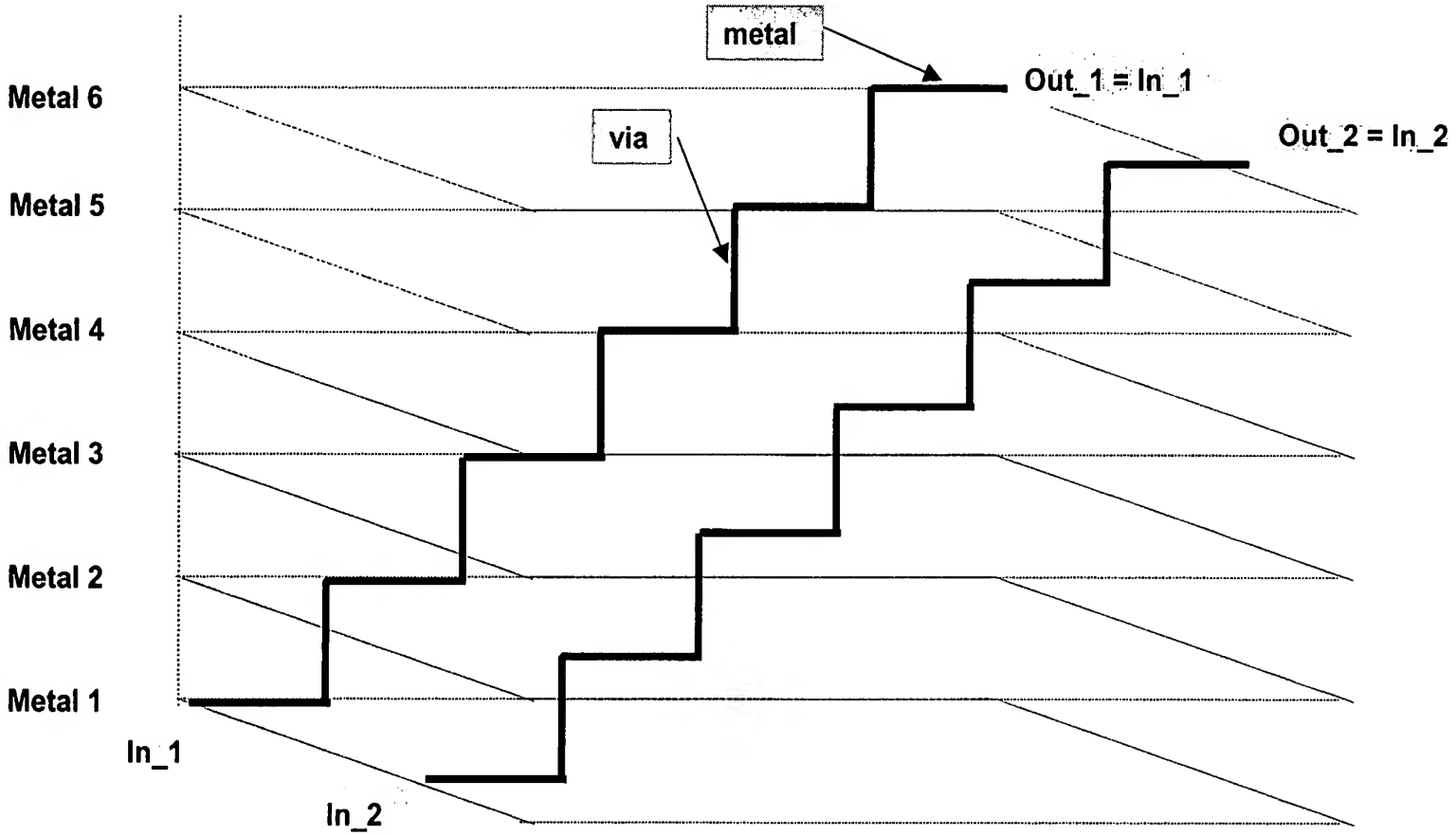

metal
Out_1 = In_1
via
Out_2 = In_2
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
In_1
In_2

FIG. 28

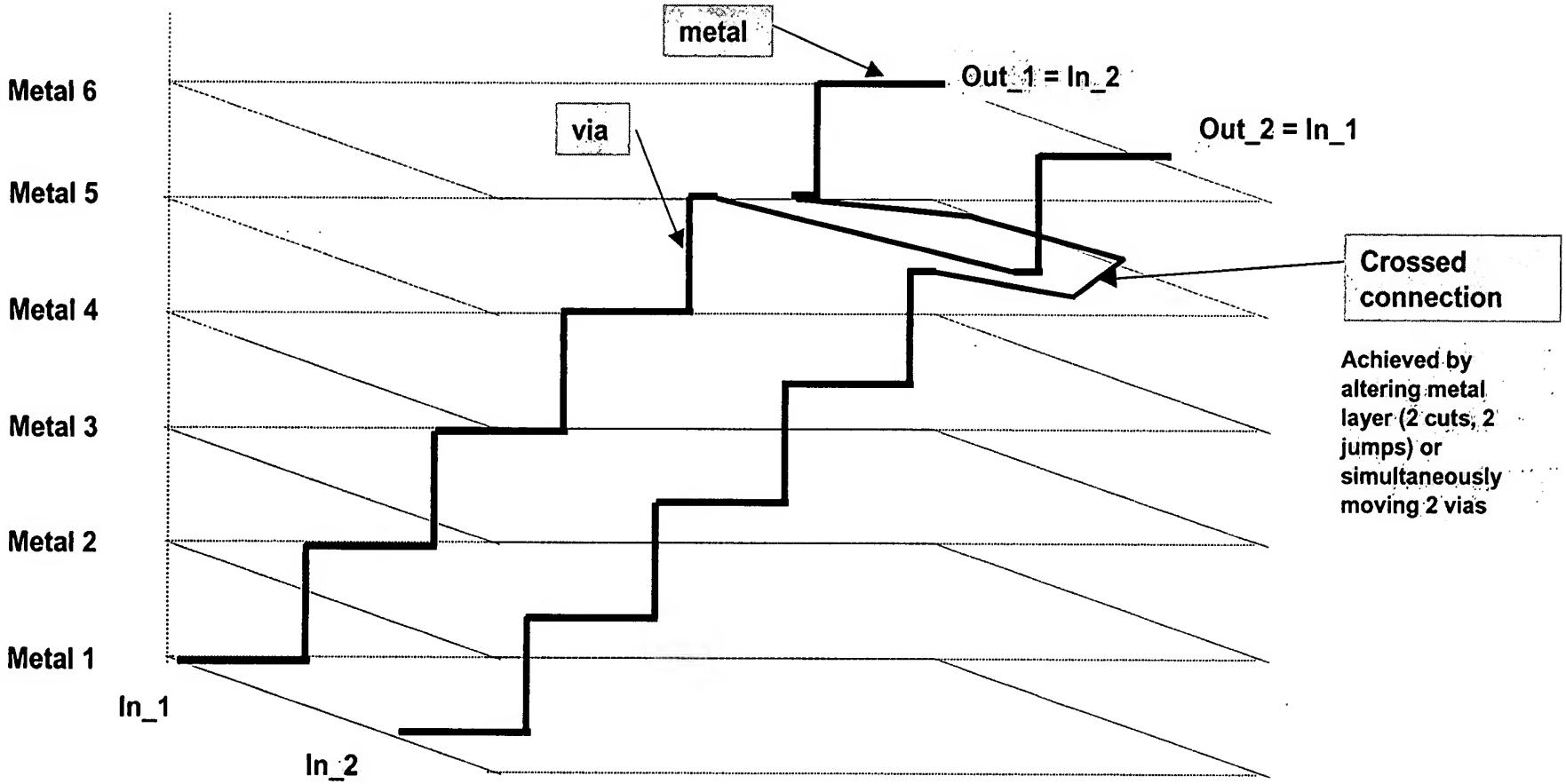

metal
Out_1 = In_2
via
Out_2 = In_1
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
In_1
In_2
Crossed connection
Achieved by altering metal layer (2 cuts, 2 jumps) or simultaneously moving 2 vias

FIG. 29

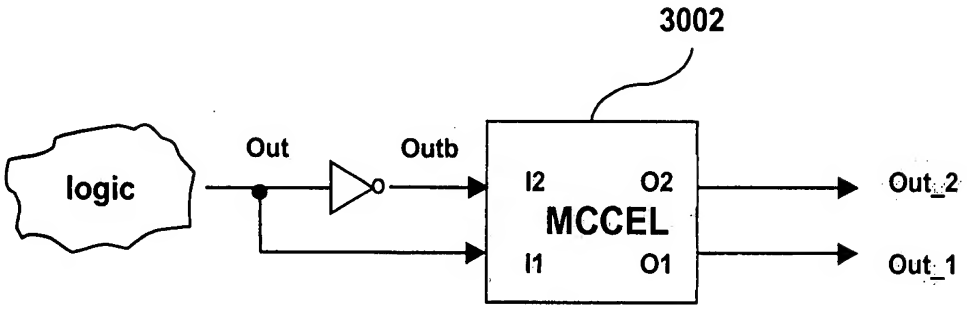


FIG. 30A

Out_1	Out_2	Comment
Out	Outb	Default
Outb	Out	Metal/Via Change

FIG. 30B

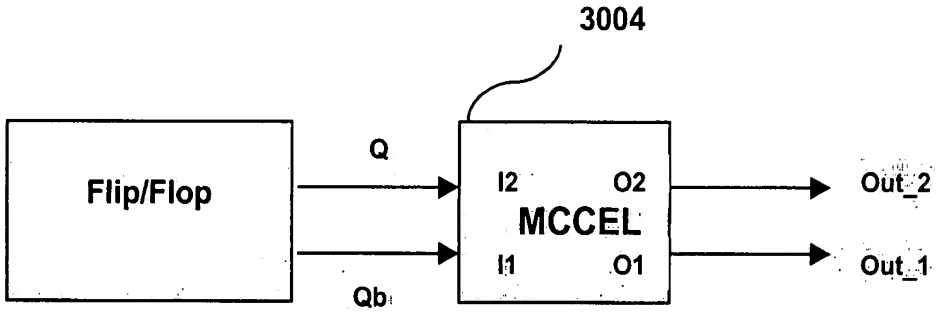


FIG. 30C

Out_1	Out_2	Comment
Q	Qb	Default
Qb	Q	Metal/Via Change

FIG. 30D

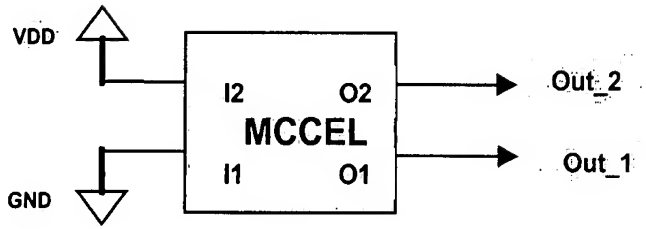


FIG. 31A

Out_1	Out_2	Comment
0	1	Default
1	0	Metal/Via Change

FIG. 31B

In_2

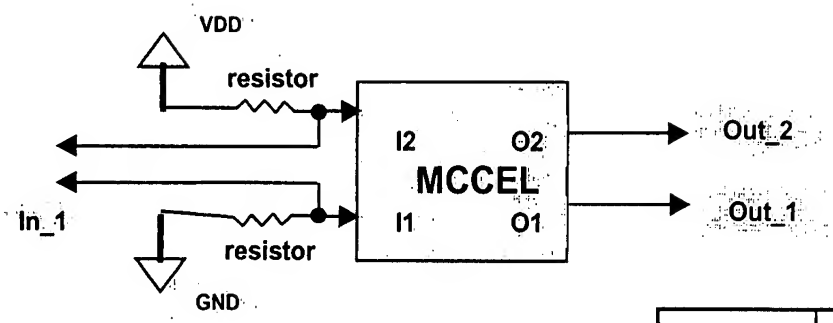


FIG. 31C

Out_1	Out_2	Comment
weak '0'	weak '1'	Default (In_1 & In_2 floating)
weak '1'	weak '0'	Metal/Via Change (In_1 & In_2 floating)
in_1	in_2	Default (In_1 & In_2 driven)
in_2	in_1	Metal/Via Change (In_1 & In_2 driven)

FIG. 31D

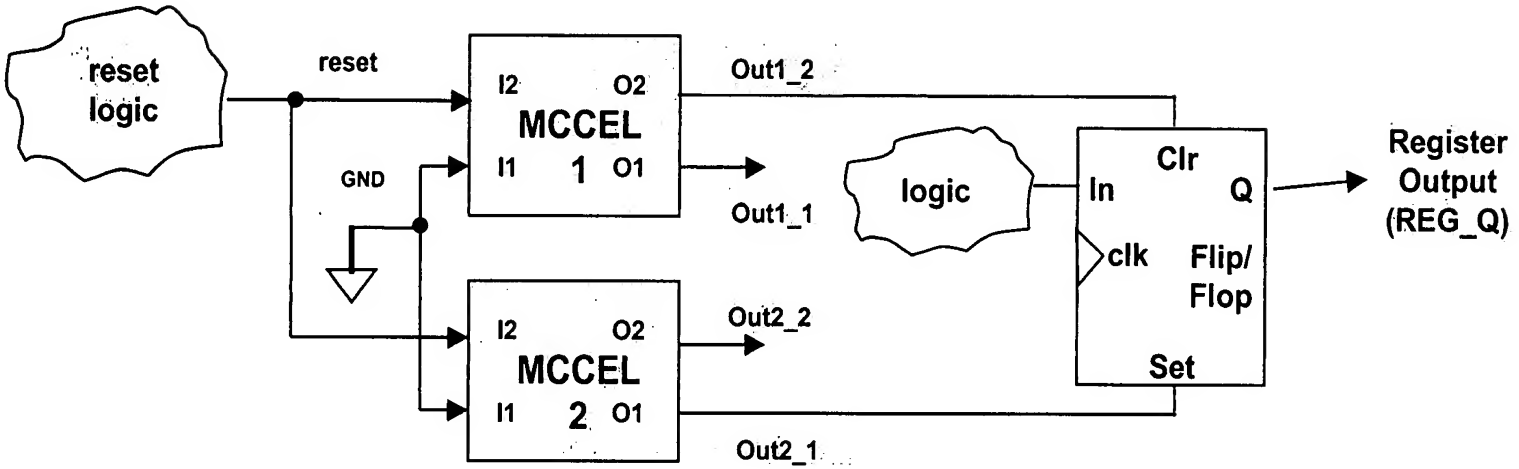


FIG. 32A

Reset	MCCEL1	MCCEL2	Reg Q
0	0	0	Q
0	0	1	Q
0	1	0	Q
0	1	1	Q
1	0	0	0
1	0	1	X
1	1	0	X
1	1	1	1

FIG. 32B

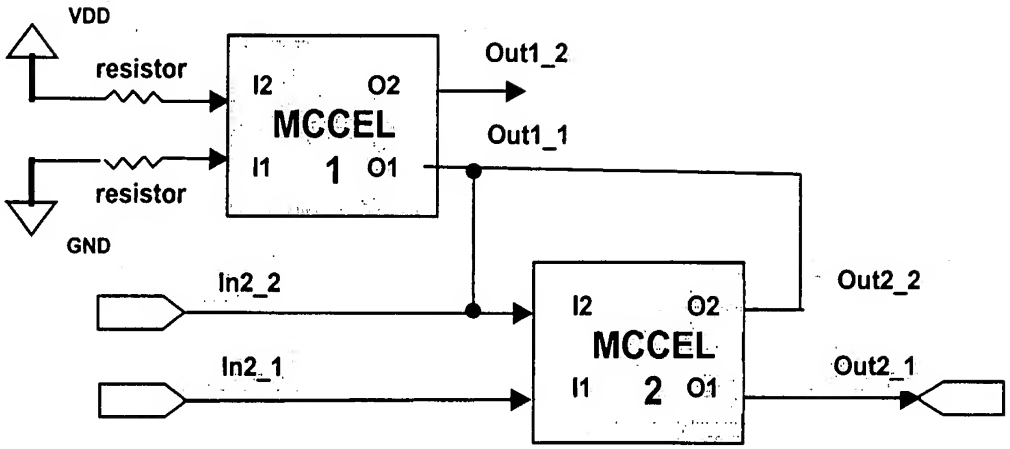


FIG. 33A

MCCEL1	MCCEL2	Out2_1
0	0	In2_1 (default)
0	1	In2_1 + In2_2 + pull-down
1	0	In2_1
1	1	In2_1 + In2_2 + pull-up

FIG. 33B

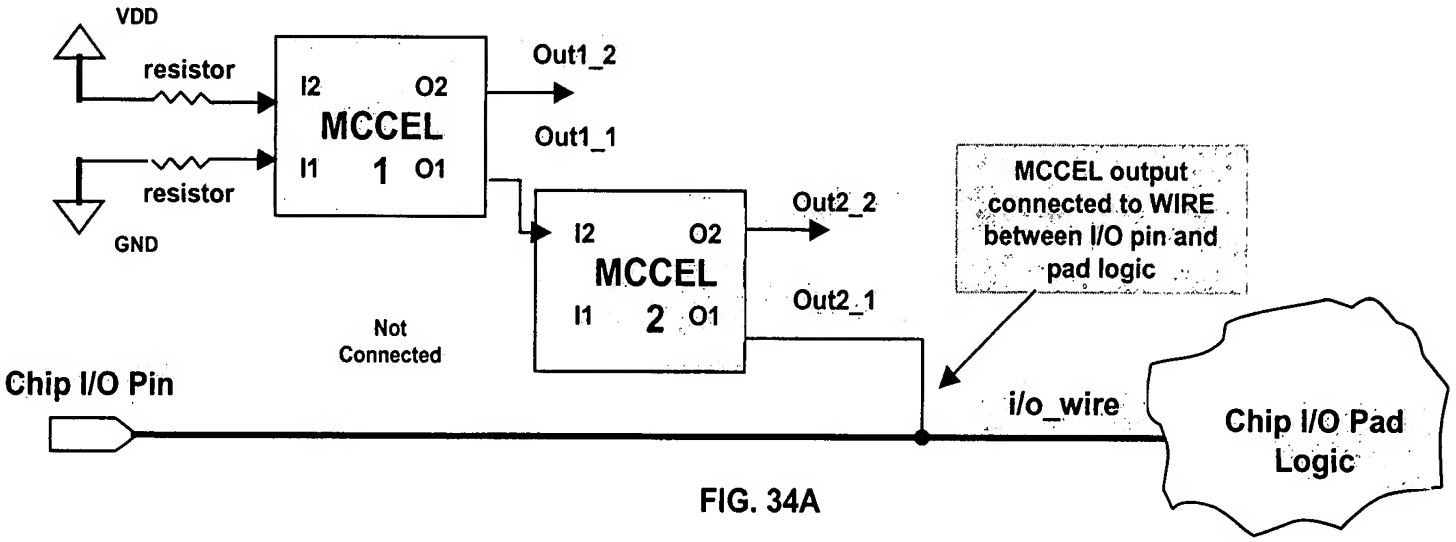


FIG. 34A

MCCEL1	MCCEL2	I/O_Pin
0	0	i/o_wire (default)
0	1	I/o_wire + pull-down
1	0	i/o_wire
1	1	i/o_wire + pull-up

FIG. 34B

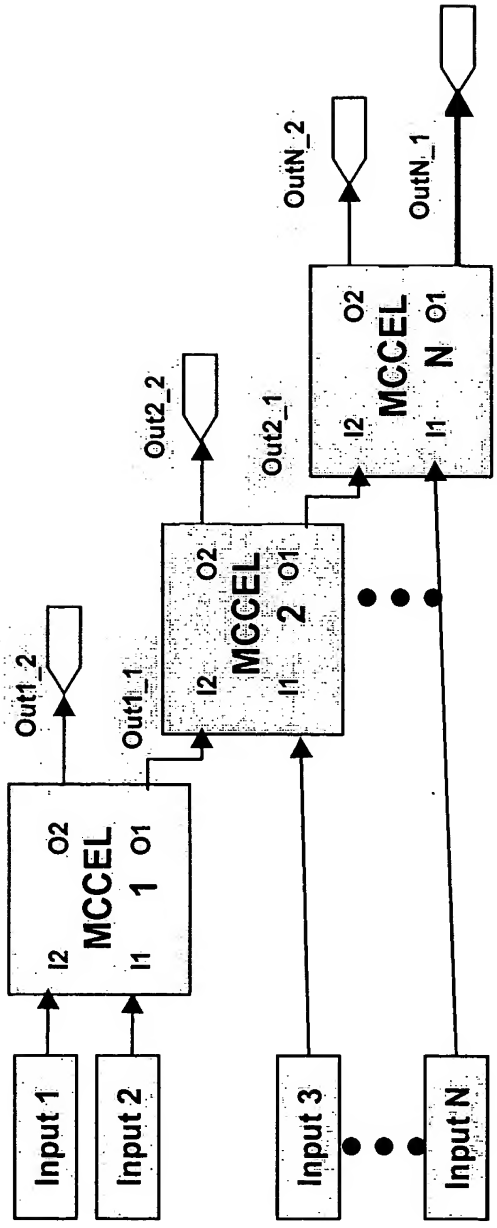

Input 1
Input 2
Input 3
Input N
MCCEL 1
MCCEL 2
MCCEL N
I1
I2
O1
O2
Out1_1
Out1_2
Out2_1
Out2_2
OutN_1
OutN_2

FIG. 35

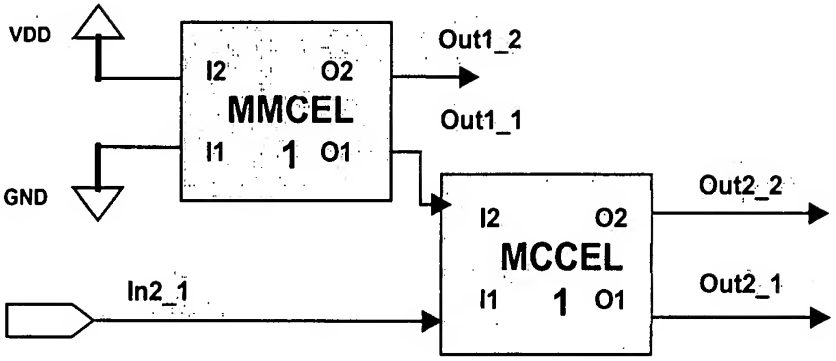


FIG. 36A

MMCEL1	MCCEL1	Out2_1	Out2_2
0	0	In2_1 (default)	0 (default)
0	1	0	In2_1
1	0	In2_1	1
1	1	1	In2_1

FIG. 36B

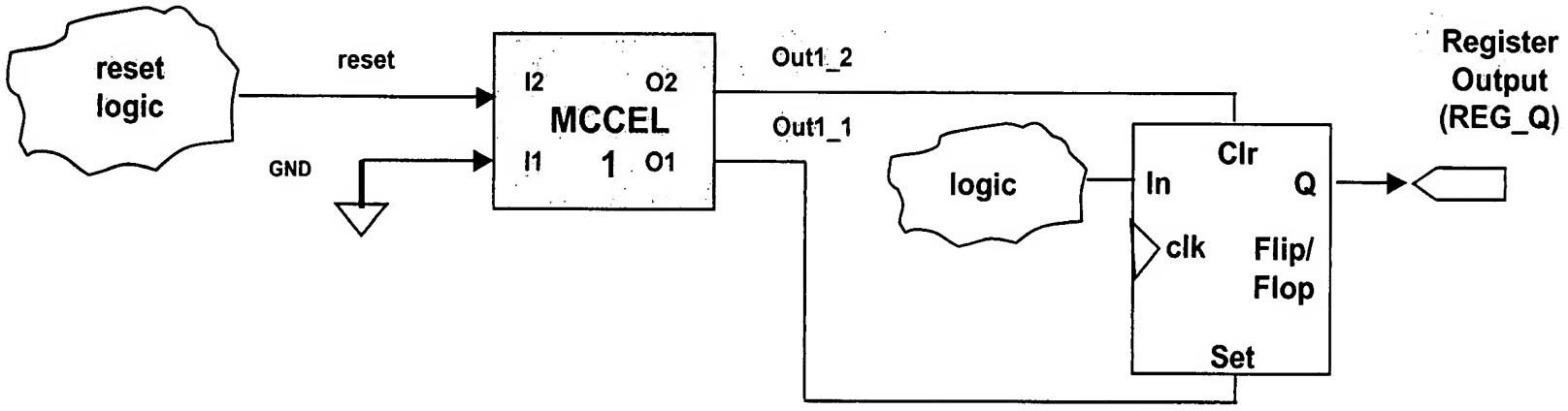


FIG. 37A

Reset	MCCEL1	Reg_Q
0	0	Q
0	1	Q
1	0	0
1	1	1

FIG. 37B